Netra™ CP3020 Board User's Guide

Sun Microsystems, Inc.
www.sun.com

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Contents

Tables

Figures

Preface

The *Netra CP3020 Board User's Guide* describes the hardware specifications, function, and physical properties of the Netra™ CP3020 board. It also provides detailed information on the system firmware. The *Netra CP3020 Board User's Guide* is written for system integration engineers, field applications and service engineers, and others involved in the integration of this board into systems. This guide is written for personnel who are familiar with the Solaris™ Operating System, the MontaVista Carrier Grade Linux operating system, and Advanced Telecommunications Computing Architecture (ATCA) computing environment.

How This Document Is Organized

Chapter 1 provides an overview of the Netra CP3020 board.

Chapter 2 provides instructions on hardware installation.

Chapter 3 provides information on the supported operating systems and on the Sun Validation Test Suite (SunVTS) software.

Chapter 4 provides information on the Netra CP3020 firmware.

Chapter 5 provides information on hardware architecture.

Appendix A provides information on the Netra CP3020 physical characteristics.

Appendix B provides first-level and second-level BIOS menu illustrations.

Appendix C provides BIOS POST codes.

Using UNIX Commands

This document might not contain information about basic UNIX® commands and procedures such as shutting down the system, booting the system, and configuring devices. Refer to the following for this information:

- Software documentation that you received with your system
- Solaris Operating System documentation, which is at:

  http://docs.sun.com

Shell Prompts

Shell	Prompt
C shell	*machine-name*%
C shell superuser	*machine-name*#
Bourne shell and Korn shell	$
Bourne shell and Korn shell superuser	#

Typographic Conventions

Typeface*	Meaning	Examples
`AaBbCc123`	The names of commands, files, and directories; on-screen computer output	Edit your `.login` file. Use `ls -a` to list all files. `% You have mail.`
`AaBbCc123`	What you type, when contrasted with on-screen computer output	`% su` `Password:`
AaBbCc123	Book titles, new words or terms, words to be emphasized. Replace command-line variables with real names or values.	Read Chapter 6 in the *User's Guide*. These are called class options. You must be superuser to do this. To delete a file, type `rm` *filename*.

* The settings on your browser might differ from these settings.

Related Documentation

For additional information about the Netra CP3020 board or the Netra CP30X0 rear transition module, refer to the following documents.

Title	Part No.
Netra CP3020 Board User's Guide (this manual)	819-4962
Netra CP3020 Board Getting Started Guide	819-4876
Netra CP3020 Board Product Notes	819-4961
Netra CP3020 Board Safety and Compliance Guide	819-4960
Netra CP30X0 Rear Transition Module Getting Started Card	819-1186
Netra CP30X0 Rear Transition Module User's Guide	819-1187
Important Safety Information for Sun Hardware Systems	816-7190
OpenBoot PROM Enhancements for Diagnostic Operation	817-6957

Documentation, Support, and Training

Sun Function	URL
Documentation	http://www.sun.com/documentation
Support	http://www.sun.com/support
Training	http://www.sun.com/training

Except for the *Important Safety Information for Sun Hardware Systems*, all the documents listed are available online at:

http://www.sun.com/documentation

Third-Party Web Sites

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Please include the title and part number of your document with your feedback:

Netra CP3020 Board User's Guide, part number 819-4962

CHAPTER 1

Introduction to the Netra CP3020 Board

This chapter provides an overview of the features, configurations, and system requirements of the Netra CP3020 board.

This chapter contains the following sections:

1.1 Overview

The Netra™ CP3020 board is a high-performance, single-board computer based on an AMD Opteron X64 processor, and is designed for high availability in a switched network computing environment. This board is compliant with Advanced Telecommunications Computing Architecture (ATCA) specifications (PICMG 3.0 and PICMG 3.1). It can achieve greater performance levels than previously supported CompactPCI® (cPCI) standards-based products targeted for Telco markets.

The PCI Industrial Computer Manufacturers Group (PICMG) standards committee has developed a new standard called ATCA or PICMG 3.x to address the issues in its previous standards, which are based on cPCI and CompactPCI Packet Switching Backplane (cPSB) (PICMG 2.x). The PICMG 3.x standard incorporated the following changes to the existing PICMG 2.x family of products:

- Larger board space, 8 rack units (8U) compared to 6U for cPCI, which allows more features and processing power

- On-board power supplies deriving local power from redundant -48V from the backplane (rather than separate power supplies)
- 6 HP slot width, which allows greater component height and new mezzanine card options
- Elimination of PCI connectivity between the boards in the system and reallocation of connectivity to serial interconnects, which eliminates single point of failure in the system
- Mandatory use of Intelligent Platform Management Interface (IPMI) management interfaces
- Flexible user I/O
- Power and thermal management guidelines enforced by management infrastructure
- Separation of control and data traffic by supporting Base Fabric (PICMG 3.0) and Extended Fabric (PICMG 3.1)

The ATCA standard comprises the PICMG 3.0, 3.1, 3.2, and 3.3 versions of the standard. The Netra CP3020 board complies with the following specifications:

- PICMG 3.0, the base specification that defines the mechanical, power distribution, system management, data transport, and regulatory guidelines
- PICMG 3.1, which builds on the PICMG 3.0 base specification and on IEEE 802.3-2003

1.2 Features

The Netra CP3020 board supports two 10/100BASE-T Ethernet interfaces as Base Fabric (requirement of PICMG 3.0) and two ports of serializer/deserializer (SERDES) Gigabit Ethernet interfaces (PICMG 3.1) as an Extended Fabric interface. The Base Fabric is used as the control interface, and the Extended Fabric can be used for data traffic. Both Base and Extended Fabric interfaces are configured as Dual Star configurations.

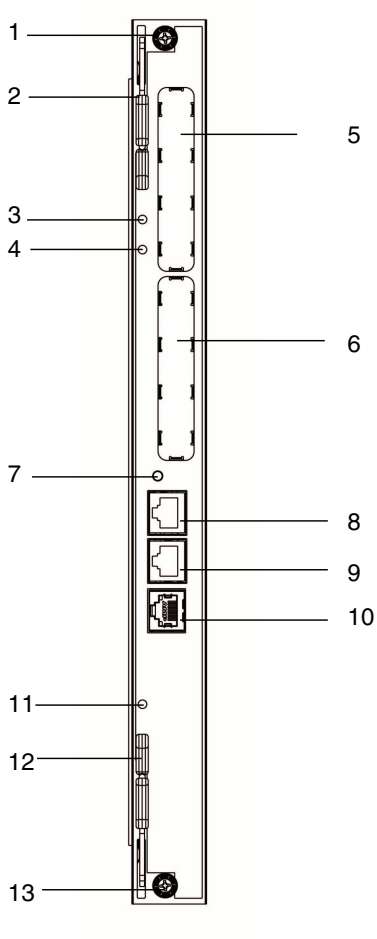
The Netra CP3020 board features include:

- One single-core or dual-core, AMD Opteron processor
- Double Data Rate (DDR-1) DIMMs, up to 8 Gbytes (very low-profile DIMMs)
- Two PCI telecom mezzanine card (PMC) expansion slots that support PCI I/O expansion and storage PMC modules

Caution – Use only 3.3V PMC cards. PMC cards are keyed so that only the 3.3V cards can be inserted onto the Netra CP3020 board. Do not disable the keying posts on 5V PMC cards to try and install them on the Netra CP3020 board.

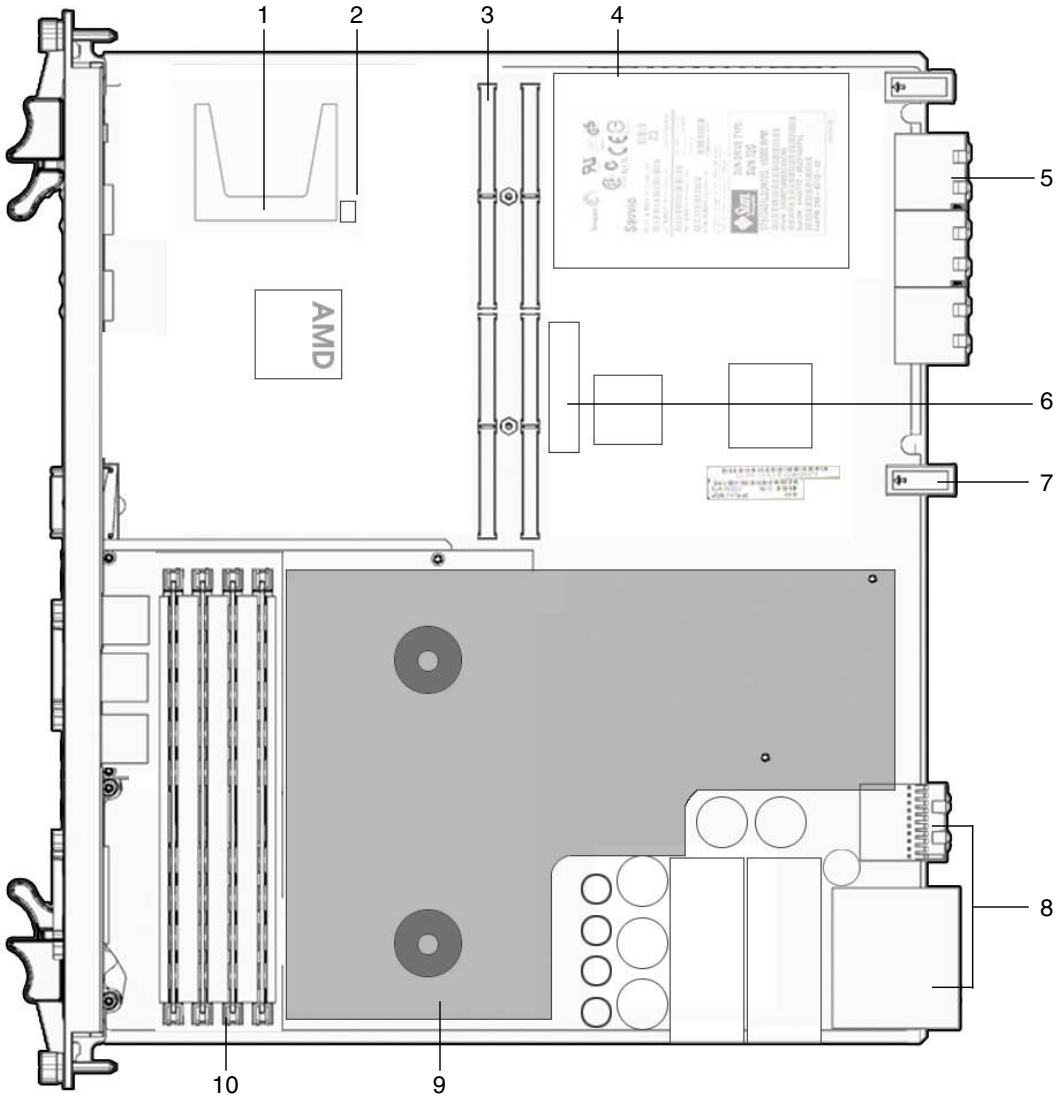
- Two-channel Serial Attached SCSI (SAS) port for external storage access
- Two 10/100BASE-T Ethernet interfaces as maintenance ports
- One asynchronous serial port
- Compact Flash socket to support up to 2-Gbyte user flash Type I
- Up to two on-board SAS drives
- Management support using Pigeon Point Systems controller (IPMC) to provide a redundant IPMI channel to communicate with the shelf manager
- Rear I/O access using a compatible rear transition module

FIGURE 1-1 and FIGURE 1-2 show a typical Netra CP3020 board, and TABLE 1-1 summarizes the features of the board



1 Captive screw
2 Top latch
3 Out-of-Service LED (Yellow)
4 OK LED (Green)
5 PMC A
6 PMC B
7 Reset button
8 Ethernet A
9 Ethernet B
10 Serial console
11 Hot-Swap LED
12 Bottom latch/hot-swap latch
13 Captive screw

FIGURE 1-1 Netra CP3020 Board (Front View)



1. Compact flash location
2. Jumper 3 location
3. PMC connectors (2 sets of 4)
4. SAS disk drive (optional)
5. Zone 1 connectors
6. SAS disk drive slot
7. Zone 2 connectors
8. Zone 3 connectors
9. Heatsink
10. DIMMs

FIGURE 1-2 Netra CP3020 Board (Component Side)

TABLE 1-1 Feature Summary

Feature	Description
CPU	• One single-core or dual-core AMD Opteron processor • Single-core CPU speed: 2.2 GHz • Dual-core CPU speed: 1.8 GHz
Memory	• 4 DDR-1 184-pin very low-profile DIMMs, buffered and registered • 1-Gbyte or 2-Gbyte DIMMs for a total memory of 4 or 8 Gbytes for 2P configurations • ECC supported
Power requirement	Supports ATCA 3.0 standard of 200 watts maximum
PICMG and PMC compliance	• PICMG 3.0 R1.0 • PICMG 3.1 R1.0 • PMC IEEE P1386.1/Draft 2.3 • PICMG 2.15 R1.0 (PTMC standard)
Node board support	Functions as a CPU node board supporting the Solaris 10 Operating System or MontaVista Carrier Grade Linux
Operating system	• Solaris 10 Operating System • MontaVista Carrier Grade Linux
Internal I/O (connections to backplane)	• Dual Gigabit Ethernet for Base Fabric interface • Dual SERDES interface as Extended Fabric interface • Dual IPMI channel connects to the backplane for communicating with shelf management

TABLE 1-1 Feature Summary *(Continued)*

Feature	Description
External I/O	• Two 10/100-Mbits per second Ethernet ports for maintenance (front or rear) • One asynchronous serial port, one on the front and one on the rear • Two 2X SAS ports (located on board); speed: 300 Mbytes/sec per channel • Rear access support using Netra CP30X0 rear transition module –Netra CP3020 front I/O is redirected to rear when rear transition module is present. –Serial port access is available in front and rear when rear transition module is present. Access is available only in front when no rear transition module is present. –2X SAS port is available only when rear transition module is installed. • PMC I/O rear access needs corresponding processor in PMC I/O module –Majority of PMC I/Os are routed to rear transition module as single-ended signals. –Others are routed as differential pairs to support certain Fibre Channel PMC cards.
IPMI system management	Uses IPMI communications with baseboard management controller (BMC); performs advanced system monitoring (ASM) on local board interface, for example, temperature sense, field-replaceable unit identification (FRU ID), and control
Hot-swap support	Basic, full, and high-availability (HA) hot-swap support
Front panel access	• One serial port (RJ-45 Netra/Cisco pinout) • Two 10/100BASE-T Ethernet ports (RJ-45) • Two PMC I/O access slots • Recessed Reset push button
PMC I/O	Provision for adding up to two independent hardware vendor (IHV) supplied PMC expansion ports on the front panel
NVRAM	8-Kbyte nonvolatile Inter-Integrated Circuit (I^2C) serial electrically erasable programmable ROM (EEPROM) to save OpenBoot PROM configuration
System flash	1 Mbyte on board
Building compliance	Network Equipment Building Systems (NEBS) Level 3

Note – For electromagnetic interference (EMI) compliance of front access ports, use shielded cables on all I/O ports. The shields for all shielded cables must be terminated on both ends.

1.3 Netra CP3020 Board System Configurations

Netra CP3020 boards can be installed into an ATCA shelf (chassis), as shown in FIGURE 1-3. The boards can be deployed in various electrical configurations to suit user requirements. For example, the board can be configured to boot from a network as a diskless client with either a front panel or rear transition module network connection, or from an optional Compact Flash card. Alternatively, you can install one or two SAS disks, available from IHVs, to provide local disk I/O. These disks can be used optionally as a boot path. The Netra CP3020 board has fixed on-board memory and connectors for additional memory.

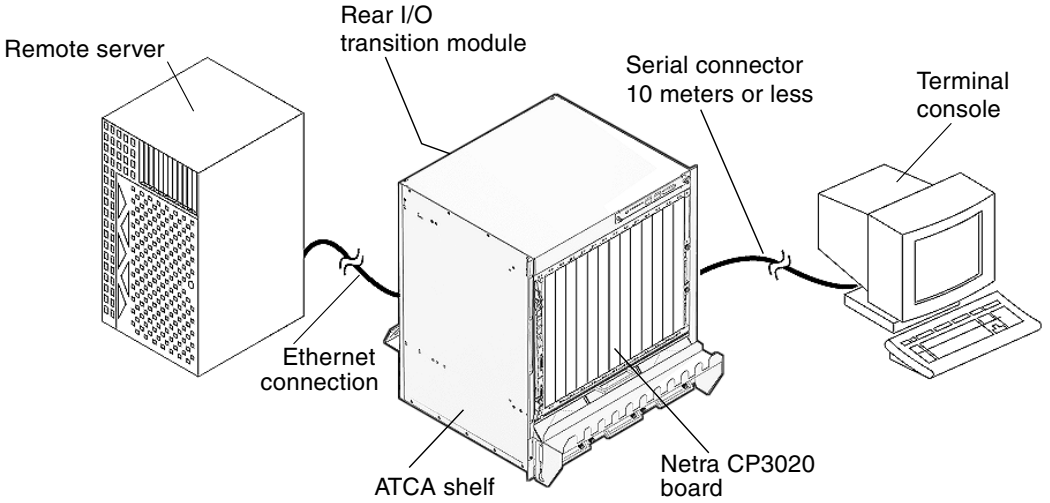


FIGURE 1-3 Netra CP3020 Board in Shelf Enclosure

1.3.1 PMC and PIM Modules

The Netra CP3020 board has two PMC slots to provide additional I/O to the front panels or to the rear of the enclosure when used with a rear transition module. A PCI Interface Module (PIM) card enables rear I/O functions when paired with a PMC card installed on the front panel of the board. PIM hardware kits are available from IHVs.

PMC cards decode their custom I/O from the Netra CP3020 board's on-board PCI bus A signals. See Section A.4.2, "PMC Connectors" on page A-7 for more information.

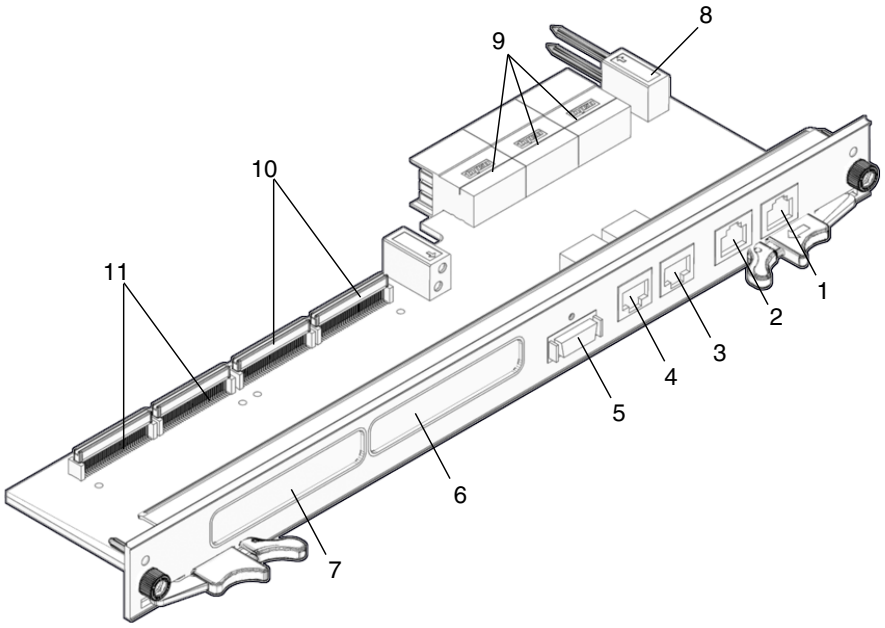
1.3.2 Rear Transition Module

You can install the optional Netra CP30X0 rear transition module (FIGURE 1-4) into the rear of the ATCA shelf, opposite the Netra CP3020 board (FIGURE 1-5). The rear transition module provides the following components:

- Two serial ports
- Two 10/100-Mbps Ethernet ports with RJ-45 connectors
- One two-channel SAS port, to its rear-panel flange (FIGURE 1-4)

Note – When a rear transition module is installed and paired with a Netra CP3020 board, the Serial B port on the rear transition module is intentionally non-functional.

Note – There are two jumper positions on the rear transition module that are configured in the factory and should not be changed. Refer to the *Netra CP30X0 Rear Transition Module User's Guide* for further details.



1 - Serial port A (RJ-45)
2 - Serial port B (RJ-45)
3 - Ethernet port A (RJ-45)
4 - Ethernet port B (RJ-45)
5 - SAS port (2x)
6 - PIM B cutout
7 - PIM A cutout
8 - Alignment pin
9 - Zone 3 connectors
10 - PIM B connectors
11 - PIM A connectors

FIGURE 1-4 Netra CP30X0 Rear Transition Module

Note – Use only serial cables that are less than 10 meters in length.

FIGURE 1-5 shows the physical relationship between the Netra CP3020 board, the rear transition module, and the backplane in a typical ATCA system.

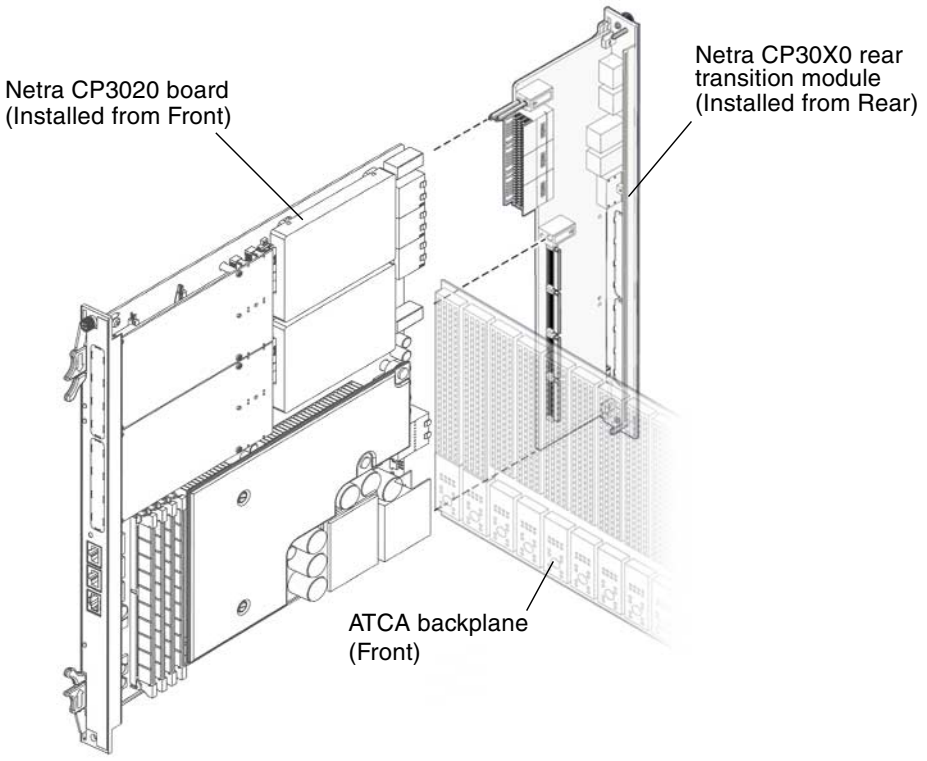


FIGURE 1-5 Netra CP3020 Board, Backplane, and Rear Transition Module Relationship

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Note – When using the rear transition module with the Netra CP3020 board, use shielded cables of less than 10 meters in length for serial I/O ports. All shielded cables must be terminated on both ends. You can use unshielded cables on Ethernet ports to satisfy EMI compliance standards.

A PIM is an extension card added to the rear transition module using the PIM slots (FIGURE 1-4). A PIM hardware kit includes a card for the PMC slot on the front panel of the Netra CP3020 board and a card for the PIM slot on the rear transition module. Note that when the PIM I/O is configured, the front PMC I/O output is not accessible.

You can order the CP30X0 rear transition module, build a custom module, or buy one from an IHV. You must set up a minimal set of I/O for a boot path for the host board and for a path for console I/O to deliver commands and read board and system status.

Possible boot and console configurations are described in TABLE 1-2. Sun Microsystems provides the Netra CP3020 board and a compatible Netra CP30X0 transition module. This transition module provides two 10/100-Mbits per second Ethernet RJ-45 ports from the host to the rear of the system. These ports can be used to accomplish optionally a network boot as a diskless client. The other configurations require IHV hardware.

TABLE 1-2 I/O Configurations

I/O	Hardware Required	Description
Ethernet	Netra CP30X0 rear transition module—supplied as an option for rear access	The default boot path uses an Ethernet port; the board runs in diskless client configuration.
SAS	Netra X4013A hard disk	The disk can be used for local boot. The optional SAS drive may also be connected via the dual SAS port on the rear transition module.
Serial data	Netra CP3020 board	Serial port A on the front panel provides the path of the default console I/O.
	Netra CP30X0 rear transition module	When the optional transition module is installed, the module's serial port A will become the path of the default console I/O (FIGURE 1-4). When a rear transition module is installed and paired with a Netra CP3020 board, the Serial B port on the rear transition module is intentionally non-functional.
Compact Flash	IDE Compact Flash card	Netra CP3020 supports one IDE Compact Flash drive up to a maximum capacity of 2 Gbytes. One Type II CF socket is provided on the board.

1.4 Hot-Swap Support

This section briefly discusses the hot-swap support on the Netra CP3020 board.

In general, the hot-swap process includes the orderly connection of the hardware and software. The process uses hardware connection control to connect the hardware in an orderly sequence. The process includes the use of pins of different lengths to accomplish signal sequencing to protect the hardware and avoid corrupting the system interface. For further details on hot-swap standards, see the ATCA hot-swap specification.

The ATCA specification describes three hot-swap models: basic hot-swap, full hot-swap, and HA hot-swap. When a Netra CP3020 board functions as a node board it supports all three hot-swap models.

1.5 System Requirements

This section contains the system-level hardware and software requirements for the Netra CP3020 board.

1.5.1 Hardware Requirements

Sun Microsystems provides the following items for customer order:

- Netra CP3020 AMD Opteron node board
- Netra CP30X0 rear transition module (optional)

  The rear transition module enables rear system I/O access to the following:

  - The network
  - A boot device
  - A console terminal (FIGURE 1-3).

  The rear transition module is optional and must be ordered separately from the Netra CP3020 board. Refer to the *Netra CP30X0 Rear Transition Module User's Guide* (819-1187) for more information.

Sun Microsystems does not provide the following components that you may need in your ATCA configuration:

- Serial terminal or terminal emulation software for console output
- Cables for terminal and network connections

Note – Use only serial cables that are less than 10 meters in length.

Rear transition modules and PMCs are optional components that you may order through Sun Microsystems or its resellers. If you use PMC cards in your configuration, you also need PIM and PMC hardware.

TABLE 1-3 ATCA System and Other Minimum Requirements

Requirements	Netra CP3020 as Node Board
ATCA system enclosure for 8U boards (includes shelf, backplane, hub/switch board, shelf manager and power supply)	Yes
Console output device or serial terminal	Yes
Boot device (such as hard drive, network, or Compact Flash card)	Yes
Peripheral device for network access	Yes
IPMC (built in)	Yes

1.5.2 Software Requirements

The Netra CP3020 board supports MontaVista Carrier Grade Linux or the Solaris™ 10 Operating System (Solaris OS) and subsequent versions that may be tested for compatibility with the Netra CP3020 board.

Refer to the *Netra CP3020 Board Product Notes* (819-4961) for more Solaris Operating System information, including a list of any required Netra software patches. You can view and download the latest version of the product notes at the following web site:

http://www.sun.com/documentation

```
Refer to the MontaVista documentation for more information on
MontaVista Carrier Grade Linux.
```

1.6 Technical Support and Warranty

Should you have any technical questions or support issues that are not addressed in the Netra CP3020 board documentation set or on the technical support web site, contact your local Sun Services representative. This hardware carries a one-year return-to-depot warranty. For customers in the U.S. or Canada, please call 1-800-USA-4SUN (1-800-872-4786). For customers in the rest of the world, you can find the World Wide Solution Center nearest you at the following web site:

`http://www.sun.com/service/contacting/solution.html`

When you call Sun Services, be sure to indicate that the Netra CP3020 board was purchased separately and is not associated with a system. Please have the board identification information ready. For proper identification of the board, be prepared to give the representative the board part number, serial number, and date code (FIGURE 1-6).

1.6.1 Board Part Number, Serial Number, and Revision Number Identification

The Netra CP3020 board part number, serial number, revision number, and media access control (MAC) address label can be found on stickers located on the Netra CP3020 board (FIGURE 1-6).

The Sun barcode label provides the following information (FIGURE 1-6):

- Board part number (for example, 3753129), which is the first seven digits on the barcode label
- Board serial number (for example, 000016), which is the next six digits on the barcode label

The dash/revision/date code label provides the following information (FIGURE 1-6):

- Product dash number (for example, -01)
- Revision number (for example, REV: 01)
- Board date code (for example, 37/2006, which represents the thirty-seventh week of year 2006)

The MAC address label contains the MAC address for the board in printed and barcode form.

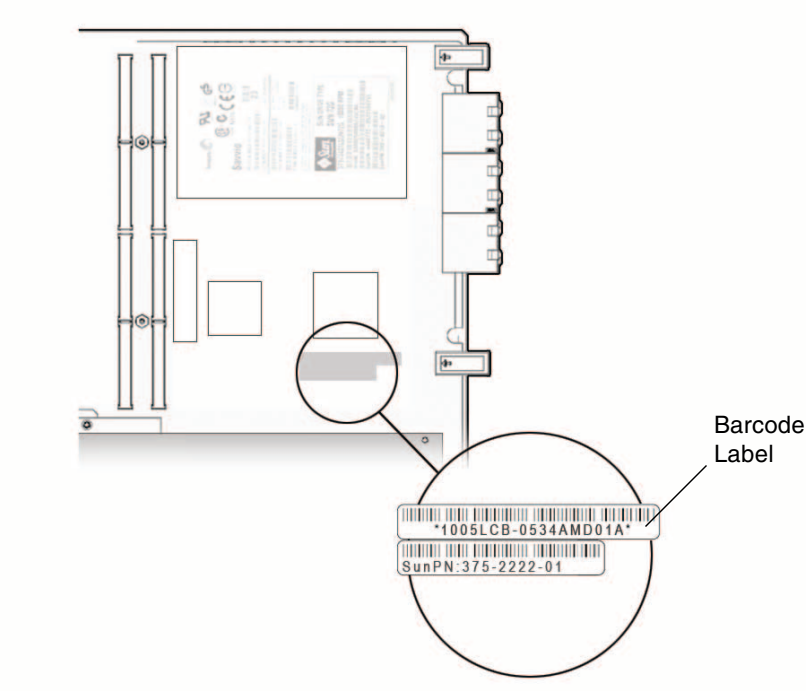


FIGURE 1-6 Netra CP3020 Board Barcode Labeling

Note – You might find the labels shown in FIGURE 1-6 on other locations on your board. Also, your particular board configuration might appear different from the illustration.

CHAPTER 2

Hardware Installation

This chapter describes the Netra CP3020 board hardware installation procedures.

This chapter contains the following sections:

2.1 Equipment and Operator Safety

Refer to the *Important Safety Information for Sun Hardware Systems* (816-7190) for general safety information.

Read the following safety statements that are specific to the Netra CP3020 board carefully before you install or remove any part of the system.

Caution – Depending on the particular chassis design, operations with open equipment enclosures can expose the installer to hazardous voltages with a consequent danger of electric shock. Ensure that line power to the equipment is disconnected during operations that make high voltage conductors accessible.

The installer must be familiar with commonly accepted procedures for integrating electronic systems and the general practice of Sun systems integration and administration. Although parts of these systems are designed for hot-swap

operation, other components must not be subjected to such stresses. Work with power connected to a shelf only when necessary, and follow these installation procedures to avoid equipment damage.

This equipment is sensitive to damage from electrostatic discharge (ESD) from clothing and other materials. Use the following antistatic measures during an installation:

- If possible, disconnect line power from the shelf when servicing a system or installing a hardware upgrade. If the shelf cannot be placed on a grounded antistatic mat, connect a grounding strap between the facility electrical input ground (usually connected to the shelf) and facility electrical service ground.
- Use an antistatic wrist strap when performing the following tasks:
  - Removing a board from its antistatic bag
  - Connecting or disconnecting boards or peripherals

  The other end of the antistatic wrist strap lead should be connected to one of the following:

  - A ground mat
  - The chassis metal as a ground

  The grounded mat or the chassis must be connected to a facility ground to prevent a floating ground.
- Keep boards in the antistatic bags until they are needed.
- Remove a board from its antistatic bag only when wearing a properly connected ground strap.
- Place circuit boards that are out of their antistatic bags on an antistatic mat if one is available and the mat is grounded to a facility electrical service ground. Do not place boards on top of an antistatic bag unless the outside of the bag also has antistatic protective properties.

2.2 Materials and Tools Required

This section provides information on the materials and tools required to install the board. The tools required for installation are:

- Phillips screwdrivers: No. 1 (required), No. 2 (optional)
- A pair of pliers or a hex driver
- Antistatic wrist strap
- Terminal console
- Serial cable of less than 10 meters in length to connect the Netra CP3020 board with a system console

Refer to Section 1.5, "System Requirements" on page 1-13 for information on hardware requirements.

2.3 Preparing for the Installation

Prepare for installation by reading and performing the following steps.

1. Become familiar with the contents of the referenced documentation.
2. Verify that all listed hardware and software are available (see Section 1.5, "System Requirements" on page 1-13).
3. Check power, thermal, environmental, and space requirements (see Section 2.3.1, "Checking Power, Thermal, Environmental, and Space Requirements" on page 2-4).
4. Verify that local area network (LAN) preparations are completed (see Section 2.3.2, "Determining Local Network IP Addresses and Host Names" on page 2-4).
5. Ensure that the host names and their network IP addresses are allocated and registered at the site.

2.3.1 Checking Power, Thermal, Environmental, and Space Requirements

Observe the following requirements:

- Your enclosure specifications can support the sum of the specified maximum board power loads.
- Facility power loading specifications can support the rack or enclosure requirements.
- Your enclosure specifications can support the cooling airflow requirements.

The Netra CP3020 board fits into a standard ATCA shelf. If your installation requirements are different, contact your field applications engineer.

2.3.2 Determining Local Network IP Addresses and Host Names

Collect the information listed in TABLE 2-1 to connect hosts to the LAN. Ask your network administrator for help, if necessary. This information is not needed for a stand-alone installation. Use TABLE 2-1 to record this information.

TABLE 2-1 Local Area Network Information

Information Needed	Your Information
IP address* and host name for each Netra CP3020 client	
Domain name	
Type of name service and corresponding name server names and IP addresses—for example DNS and NIS (or NIS+)	
Subnet mask	
Gateway router IP address	
Network File System (NFS) server names and IP addresses	
Web server URL	

* Local IP addresses are not needed if they are assigned by a network Dynamic Host Configuration Protocol (DHCP) server.

You may need the MAC (Ethernet) addresses of the local hosts to make name server database entries. You can see the MAC address in the console output while booting the board. You can also find it on the barcode label on the node board (see Section 1.6.1, "Board Part Number, Serial Number, and Revision Number Identification" on page 1-15).

2.3.3 Netinstall Boot Device

TABLE 2-2 provides a map of the MAC addresses on the Netra CP3020 board, the corresponding Solaris devices, and the interfaces on the Netra CP3020 board. You might need this information to understand which MAC address is associated with the system IP address on the install server.

For example, the extended fabric interface is connected to the DTI switch in slot 8 of the ATCA shelf. To install through this device, select the 309 Ethernet interface from the BIOS Setup menus.

TABLE 2-2 Netinstall Boot Device Connectivity

MAC Address	Broadcom BIOS Port Number Enumeration	Solaris Device	Hardware Device	Description	Connects to DTI Slot
0:3:ba.xx.xx.	208	bge0	(5704C)	Base fabric 0	slot 7
0:3:ba.xx.xx.xn+1	209	bge1	(5704C)	Base fabric 1	slot 8
0:3:ba.xx.xx.xn+2	308	bge2	(5704S)	Extended fabric 0	slot 7
0:3:ba.xx.xx.xn+3	309	bge3	(5704S)	Extended fabric 1	slot 8
0:3:ba.xx.xx.xn+4	110	bge4	(5705)	mgtB	N/A
0:3:ba.xx.xx.xn+5	N/A	amd8111s0	(8111)	mgtA	N/A

The 209 and 309 devices are generally on the switch in slot 8 of the ATCA shelf. Conversely, the 208 and 308 devices are generally on the switch in slot 7.

2.3.4 Installation Procedure Summary

This section summarizes the high-level procedures that are required to install the Netra CP3020 board. Ensure that you are familiar with the information in Section 2.4, "Configuring the Board Hardware" on page 2-6 through Chapter 3 before installing the board.

The process to set up and configure a Netra CP3020 board in a system includes the following procedures:

1. Configure the board's physical hardware. For example, install memory and PMC cards, and set switches, as necessary (Section 2.4, "Configuring the Board Hardware" on page 2-6).
2. Configure the rear transition module with PIMs, switch settings, or connector attachments, as necessary (Section 2.4.7, "Configuring the Rear Transition Module Hardware" on page 2-21).
3. Physically install the rear transition module as necessary (Section 2.5.1, "Installing a Rear Transition Module" on page 2-22).
4. Physically install the Netra CP3020 board, and any peripheral boards into the ATCA shelf Section 2.5, "Installing the Netra CP3020 Board in an ATCA Shelf" on page 2-21).
5. As the Netra CP3020 board is powering up, press F2 to interrupt the boot process. The system enters the BIOS Setup menus. Select the port where the netinstall server has been set up. See TABLE 2-2 for the available boot devices. Refer to the documentation for your operating system for instructions on setting up a netinstall server.
6. Connect the nodes to a local network. Alternatively, the board can operate as a stand-alone system without a network connection (Section 2.6, "Connecting External I/O Cables" on page 2-26).
7. If you are running the Solaris Operating System on the Netra CP3020 board, and want to verify system integrity, download and install SunVTS (Section 3.1, "Operating Systems" on page 3-1).

2.4 Configuring the Board Hardware

This section lists hardware installation and settings that might apply to your board configuration. Read and perform the procedures, as necessary, before installing the Netra CP3020 board into the ATCA shelf.

2.4.1 Installing DDR-1 DIMMs

The Netra CP3020 board supports a total of four DIMMs and the maximum memory capacity of 8 Gbytes (using four 2-Gbyte DIMMs). The Netra CP3020 board accommodates the following DIMMs and configurations:

- Four standard PC2700 DDR1-333 registered/ECC DIMMs
- DIMMs must be installed in matching pairs
- DIMM slots 0 and 1 (closest to the CPU heat sink) must always be installed
- 1-Gbyte and 2-Gbyte DDR-1 modules are supported
- DIMM pairs of different sizes are supported as long as the paired slots match in size. For example, you can install 1-Gbyte DIMMs in slots 0 and 1, and 2-Gbyte DIMMs in slots 2 and 3.

The Netra CP3020 board supports DIMMs that have the following characteristics:

- A 144-bit wide data bus (128+16 ECC) and up to 14 address bits
- 2.5V and a 1.25V reference voltage (Vtt)
- Very low profile (VLP) with a maximum height of 0.72 inch (18.3 mm)
- Four 184-pin Joint Electron Device Engineering Council (JEDEC) standard DDR DIMM slots that support PC-2700 registered/ECC DIMMs
- Maximum synchronous dynamic random access memory (SDRAM) clock frequency of 266 MHz
- Single-rank or dual-rank SDRAM DIMMs
- Support for four internal SDRAM device banks
- Maximum of 8 Gbytes
  - Peak memory bandwidth of 5.36 Gbytes per second at 166 MHz
  - SSTL_2 inputs and output

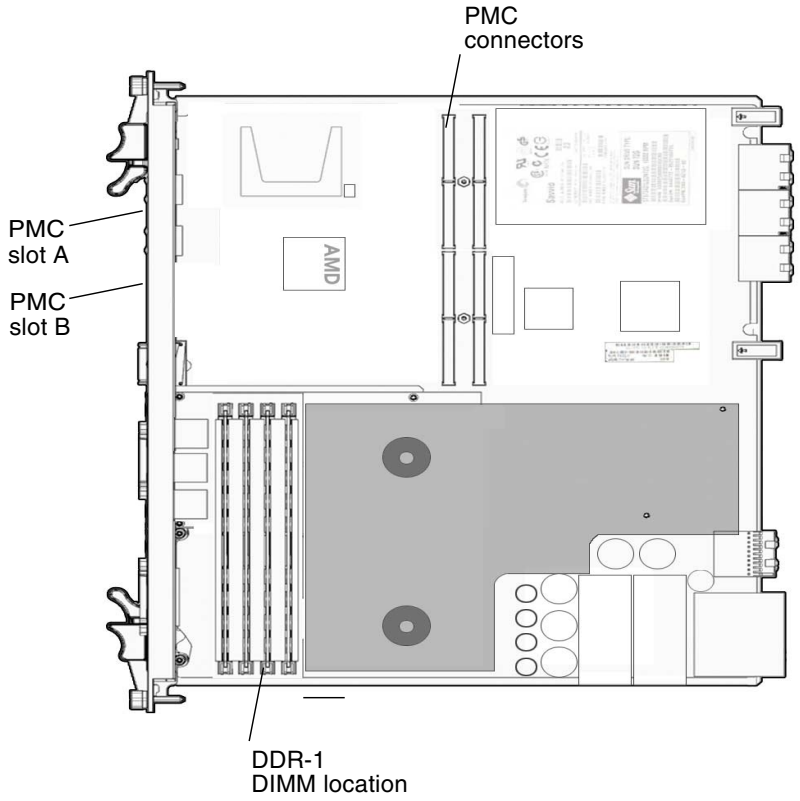


FIGURE 2-1 Location of DIMMs, PMC connectors, and PMC Slots

2.4.1.1 To Install a DDR-1 DIMM

The following procedure provides a general guide for installing additional memory. However, for specific directions on installing DIMMs on the Netra CP3020 board, refer to the documentation that shipped with the DIMMs.

1. **Perform one of the following:**
   - If the Netra CP3020 board is installed in an ATCA shelf, remove the board from the shelf as explained in Section 4.7.1, "Removing the Netra CP3020 Board" on page 4-12.
   - Remove the Netra CP3020 board from its antistatic envelope and place it on an ESD mat (if one is available) near the ATCA shelf.

     If an ESD mat is not available, you can place the board on the antistatic envelope in which it was packaged.

2. **Take antistatic precautions: Attach and electrically ground the wrist strap.**

Caution – Always wear a grounded antistatic wrist strap when handling modules.

3. **Locate the DIMM connectors on the Netra CP3020 board.**

   Select the connectors where you will install the DIMM (FIGURE 2-1). To replace an existing DIMM with a new DIMM, see Section 2.4.1.2, "To Remove a DDR-1 DIMM" on page 2-10 for instructions on removing the DIMM.

Caution – Do not remove the DIMM from its antistatic container until you are ready to install the DIMM on the Netra CP3020 board. Handle the module only by its edges. Do not touch module components or metal parts. Always wear a grounded antistatic wrist strap when handling modules.

4. **Remove the DIMM from its protective packaging, holding the module only by the edges.**

5. **Holding the DIMM upright to the board, insert the bottom edge of the DIMM into the bottom of the slot's hinge-style connector (FIGURE 2-2).**

Caution – Evenly engage the DIMM in its hinge-style slot; uneven contact can cause shorts that will damage the Netra CP3020 board. Do not rock the DIMM into place. Ensure that all contacts engage at the same time. You will feel or hear a click when the DIMM properly seats in the connector.

   The socket and module are both keyed, which means the module can be installed only one way. With even pressure, push simultaneously on both upper corners of the DIMM until its bottom edge (the edge with the gold fingers) is firmly seated in the connector.

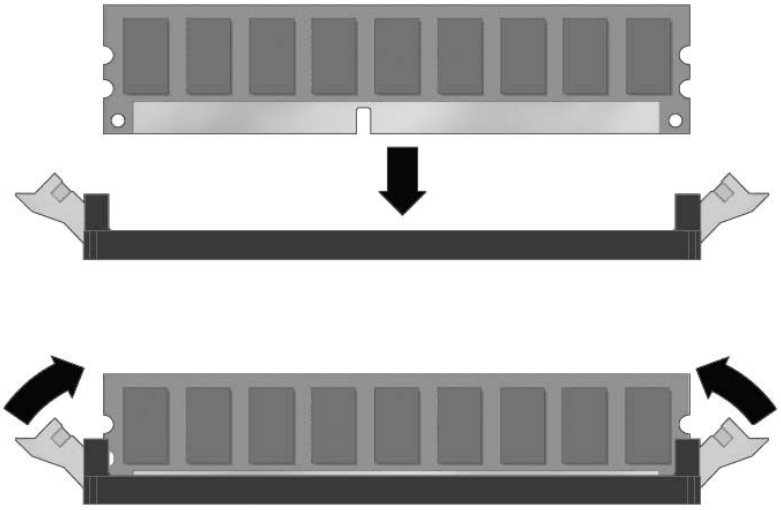


FIGURE 2-2 Installing a DIMM

6. **Press the top edge of the DIMM toward the board until the retainer clips click into place in the notches on the DIMM sides (**FIGURE 2-2**).**

   The small metal retainer clips on each side of the DIMM slot are spring-loaded, and click into place in the notches on the sides of the DIMM.

2.4.1.2 To Remove a DDR-1 DIMM

If you are returning the DIMM or the board for service or if you are replacing a DIMM with another DIMM, remove the DIMM from the Netra CP3020 board.

Note – Safely store the original factory-shipped DIMM and related DIMM packaging. Store any removed DIMM in the new DIMM packaging, or use the packaging for service.

To remove a DIMM from the Netra CP3020 board, perform the following steps:

1. **Perform one of the following:**
   - If the Netra CP3020 board is installed in an ATCA shelf, remove the board from the shelf as explained in Section 4.7.1, "Removing the Netra CP3020 Board" on page 4-12.
   - Remove the Netra CP3020 board from its antistatic envelope and place it on an ESD mat (if one is available) near the ATCA shelf.

If an ESD mat is not available, you can place the board on the antistatic envelope in which it was packaged.

Caution – Do not place boards on top of an antistatic bag unless the outside of the bag also has antistatic protective properties.

2. **Take antistatic precautions: Attach and electrically ground the wrist strap.**

Caution – Always wear a grounded antistatic wrist strap when handling modules.

3. **Simultaneously pull both spring retainer clips outward from the slot for the DIMM you want to remove.**
4. **Grasp the DIMM by the edges, and carefully pull it out of its connector. Place it in an antistatic bag.**

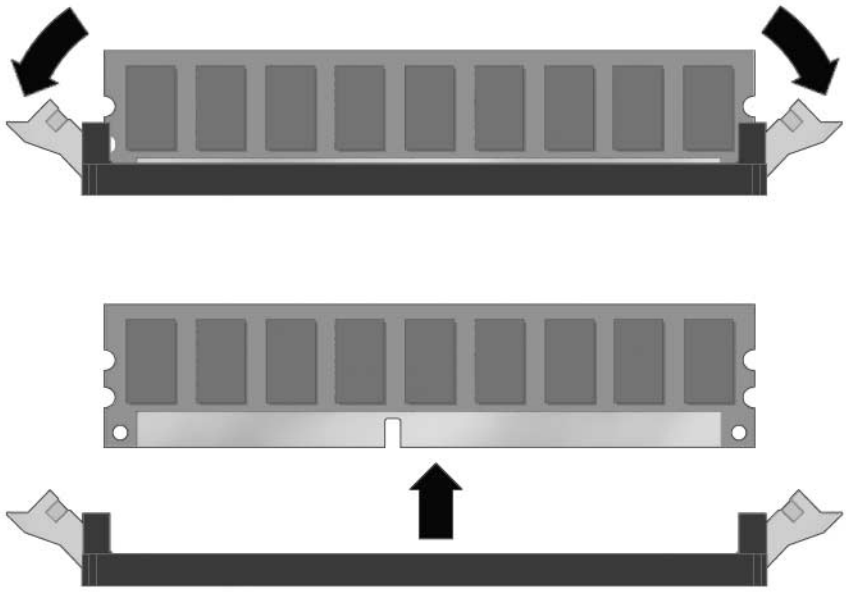


FIGURE 2-3 Removing a DIMM

5. **If you are replacing the DIMM you removed with a new DIMM, install it as described in** Section 2.4.1.1, "To Install a DDR-1 DIMM" on page 2-8**.**

Note – Before installing a replacement DIMM, verify that the new DIMM is the same size as its paired DIMM.

2.4.2 Installing the Optional TOD Battery

The Netra CP3020 board is shipped with a Time of Day (TOD) battery. The date and time stored in the TOD chip are backed up when the system is powered off. If you ever have to replace the battery, be sure to use a type CR1632 or equivalent.

1. **Perform one of the following:**
   - If the Netra CP3020 board is installed in an ATCA shelf, remove the board from the shelf as explained in Section 4.7.1, "Removing the Netra CP3020 Board" on page 4-12.
   - Remove the Netra CP3020 board from its antistatic envelope and place it on an ESD mat (if one is available) near the ATCA shelf.

     If an ESD mat is not available, you can place the board on the antistatic envelope in which it was packaged.

Caution – Do not place boards on top of an antistatic bag unless the outside of the bag also has antistatic protective properties.

2. **Slide the battery into the holder (FIGURE 2-4) with the side labeled "+" facing up.**

2.4.3 Installing the Optional Compact Flash Card

An optional IDE Compact Flash card can be installed on the Netra CP3020 board. The Compact Flash card is not hot-swappable and there is no access to the Compact Flash card once the Netra CP3020 is installed in an ATCA shelf.

1. **Perform one of the following:**
   - If the Netra CP3020 board is installed in an ATCA shelf, remove the board from the shelf as explained in Section 4.7.1, "Removing the Netra CP3020 Board" on page 4-12.
   - Remove the Netra CP3020 board from its antistatic envelope and place it on an ESD mat (if one is available) near the ATCA shelf.

     If an ESD mat is not available, you can place the board on the antistatic envelope in which it was packaged.

Caution – Do not place boards on top of an antistatic bag unless the outside of the bag also has antistatic protective properties.

2. **To install the Compact Flash card, use the arrow on the card's label as a guide and insert the card into the Compact Flash connector (FIGURE 2-4).**

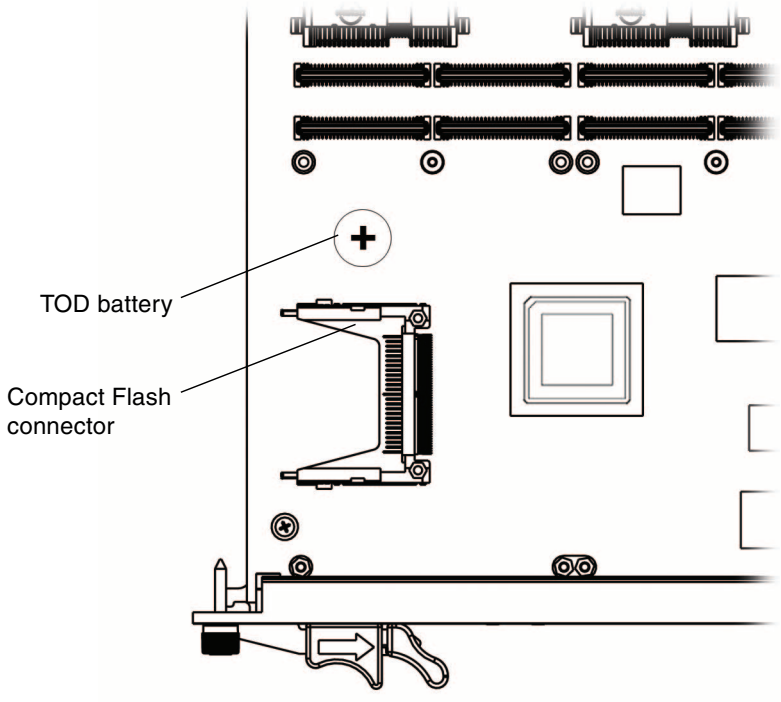


FIGURE 2-4 TOD Battery and Compact Flash Locations

2.4.4 Installing Optional PMC Cards

A PMC card is a slim, modular mezzanine card that provides additional functionality to the Netra CP3020 board. The board contains two PMC slots into which you can install optional PMC devices (FIGURE 2-1).

Note – You must install PMC cards on the Netra CP3020 board before you install the board into the ATCA shelf.

Caution – Use only 3.3V PMC cards. PMC cards are keyed so that only the 3.3V card can be inserted onto the Netra CP3020 board. Do not disable the keying posts on 5V PMC cards to try and install them on the Netra CP3020 board.

To provide rear I/O access to the PMC card, the PMC card's ship kit might contain a PIM card that must be installed on the Netra CP30X0 rear transition module. Refer to the PIM card documentation and the *Netra CP30X0 Rear Transmission Module User's Guide* (819-1187) for installation instructions.

To install an optional PMC card, follow these steps:

Note – The following procedure provides generic instructions for installing PMC cards on the Netra CP3020 board. Refer to the PMC card manufacturer's documentation for specific instructions on installing these devices.

---

1. **Retrieve the wrist strap from the adapter's ship kit.**
2. **Attach the adhesive copper strip of the antistatic wrist strap to the metal chassis. Wrap the other end twice around your wrist with the adhesive side against your skin.**
3. **Perform one of the following:**
   - If the Netra CP3020 board is installed in an ATCA shelf, remove the board from the shelf as explained in Section 4.7.1, "Removing the Netra CP3020 Board" on page 4-12.
   - Remove the Netra CP3020 board from its antistatic envelope and place it on an ESD mat (if one is available) near the ATCA shelf.

     If an ESD mat is not available, you can place the board on the antistatic envelope in which it was packaged.

Caution – Do not place boards on top of an antistatic bag unless the outside of the bag also has antistatic protective properties.

Note – If EMI compliance is required, do not remove the PMC filler panel from the Netra CP3020 board unless you are going to install a PMC card to the adapter.

---

4. **Remove the Netra CP3020 board's PMC filler panel (**FIGURE 2-5**).**

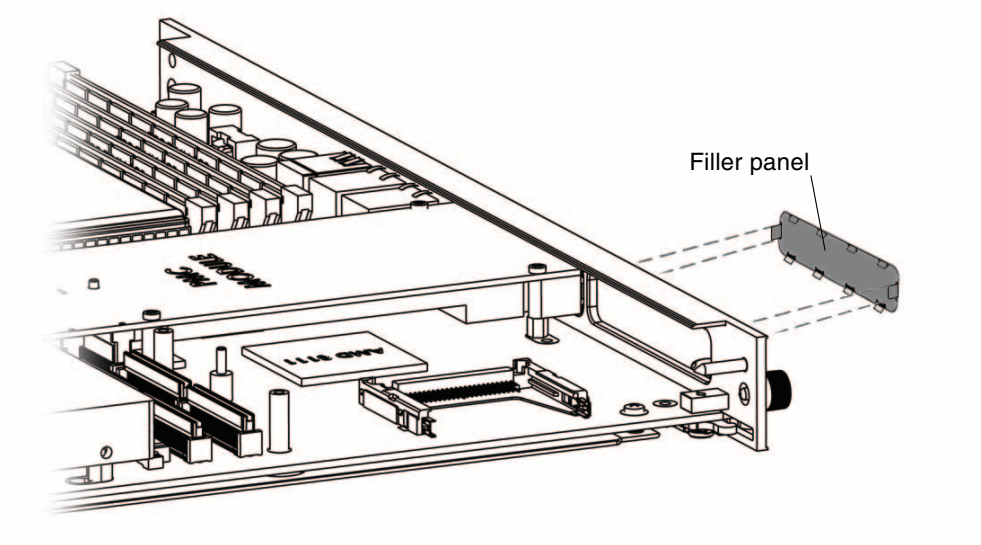


FIGURE 2-5 Removing the PMC Filler Panel

5. **Retrieve the PMC card from its ship kit and place it on an antistatic surface.**

6. **Install the standoffs on the Netra CP3020 board onto the PMC card by tightening them by hand and then tightening them a little more with a hex driver or set of pliers (**FIGURE 2-6**).**

   The standoffs, or extensions, are tube-shaped devices that support the PMC card in its raised position above the Netra CP3020 board. They are shipped with the PMC card in a small plastic bag.

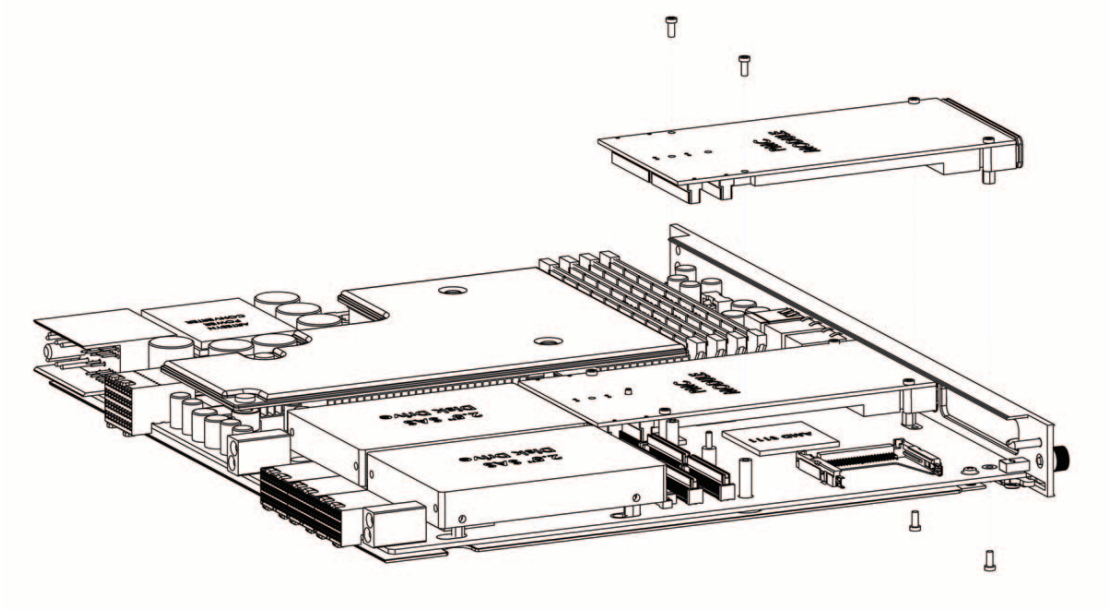


FIGURE 2-6 Installing Standoffs for the PMC Card

7. **Insert the PMC card at an angle into the appropriate PMC slot (**FIGURE 2-7**).**

   Ensure that you engage the keyhole standoffs properly, and that the PMC card slides into the correct PMC slot on the front panel.

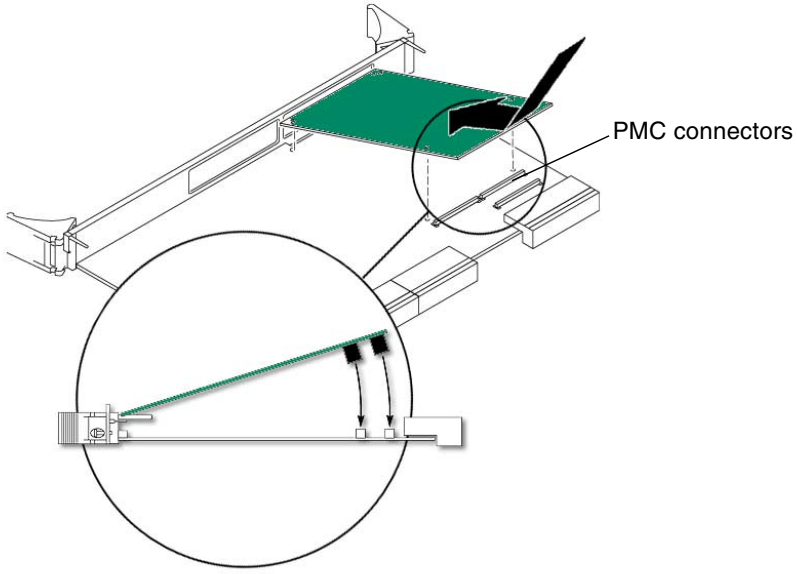


FIGURE 2-7 Installing the PMC Card

8. **Slide the PMC card forward into position and align the PMC card over the PMC connectors.**
9. **Carefully press the PMC card into the board's PMC connectors.**

Caution – Do not use excessive force when installing the PMC card into the slot. You could damage the PMC's connectors or the connectors on the Netra CP3020 board, causing permanent damage to the PMC card or the Netra CP3020 board. If the PMC card does not seat properly when you apply even pressure, remove the PMC card and carefully reinstall it.

10. **Use a screwdriver to secure the four screws that attach the PMC card to the Netra CP3020 board on the component side of the board (**FIGURE 2-8**).**

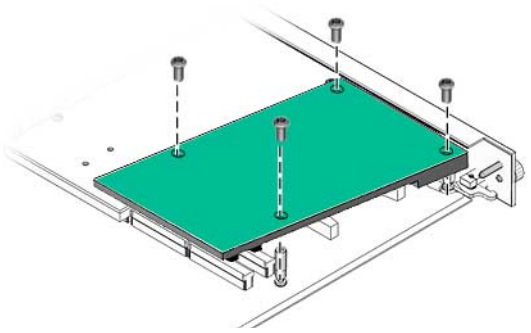


FIGURE 2-8 Securing the PMC Screws

Refer to the PMC documentation for PMC software and cabling installation instructions.

2.4.5 Installing Optional SAS Disk Drives

1. **Take antistatic precautions: Attach and electrically ground the wrist strap.**

Caution – Always wear a grounded antistatic wrist strap when handling modules.

2. **Perform one of the following:**
   - If the Netra CP3020 board is installed in an ATCA shelf, remove the board from the shelf as explained in Section 4.7.1, "Removing the Netra CP3020 Board" on page 4-12.
   - Remove the Netra CP3020 board from its antistatic envelope and place it on an ESD mat (if one is available) near the ATCA shelf.

     If an ESD mat is not available, you can place the board on the antistatic envelope in which it was packaged.

Caution – Do not place boards on top of an antistatic bag unless the outside of the bag also has antistatic protective properties.

3. **Remove the standoffs from the small plastic bag in which they ship.**

4. **Locate the disk drive locations on the Netra CP3020 board (**FIGURE 2-9**).**

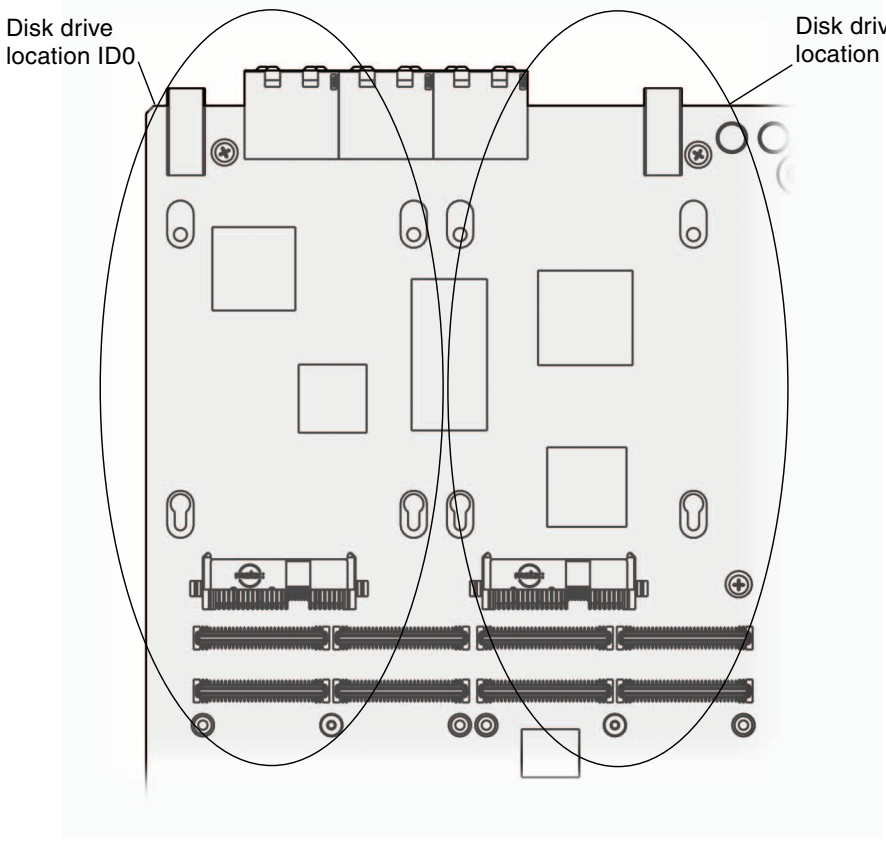


FIGURE 2-9 Disk Drive Locations on the Netra CP3020 Board

5. **Install the standoffs in the locations shown in** FIGURE 2-9**.**

6. **Install the disk drive as shown in** FIGURE 2-10**.**

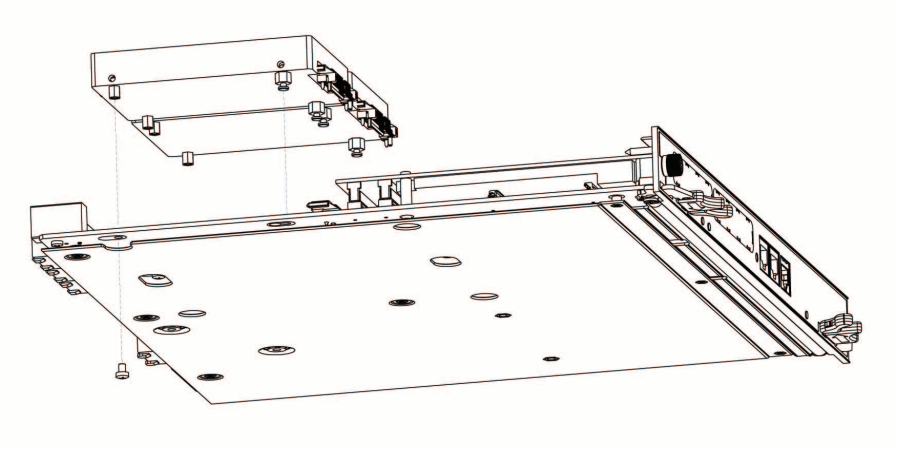


FIGURE 2-10 Installing the Optional Disk Drives

7. **Turn the Netra CP3020 board over, and use a screwdriver to secure the four screws that attach the disk drive to the Netra CP3020 board (**FIGURE 2-11**).**

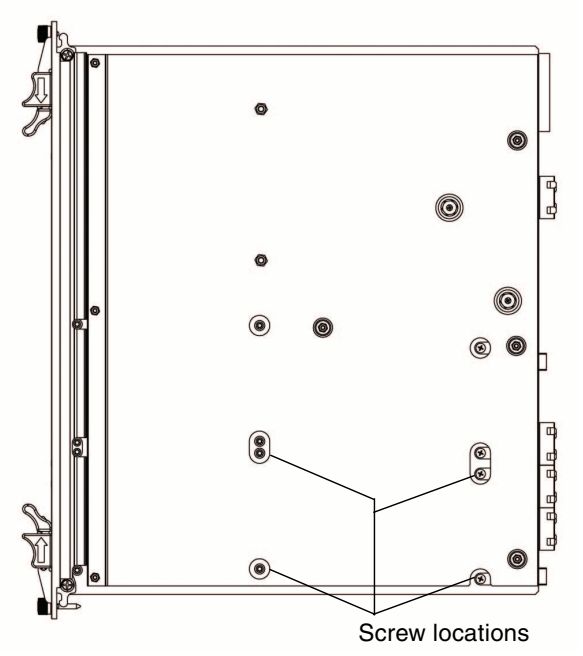


FIGURE 2-11 Securing the Disk Drive Screws

2.4.6 Setting Switches

Normally, you do not need to set or reset the switches. You also do not normally need to reset the jumpers, except in the rare case in which you need to clear the CMOS settings. See Section 4.7, "Clearing CMOS Settings" on page 4-11 for further details.

2.4.7 Configuring the Rear Transition Module Hardware

If you are using the Netra CP30X0 rear transition module, refer to the *Netra CP30X0 Rear Transition Module User's Guide* (819-1187). You can also refer to the Netra CP30X0 manual for detailed connector pin assignments.

2.4.7.1 To Install PIM Assemblies on the Rear Transition Module

Follow the PMC card manufacturer's procedure to install PIM cards. Refer to the *Netra CP30X0 Rear Transition Module User's Guide* (819-1187) for more PIM connector pin assignments and additional installation information.

Caution – When installing a PIM card onto the Netra CP30X0 module, ensure that the PIM card power signals match the corresponding power signals of the PIM connectors that are to be installed on the rear transition module.

2.5 Installing the Netra CP3020 Board in an ATCA Shelf

If you are installing the Netra CP3020 board with the rear transition module, install the rear transition module at the rear of the server and then install the Netra CP3020 board in the front of the server. Even though you will be installing the rear transition module first, look at the front of the server and locate the slot number where you will be installing the Netra CP3020 board. Then go to the back of the server and install the rear transition module in that particular slot. If you do not install the Netra CP3020 board and the rear transition module in corresponding slots, the system will recognize the Netra CP3020 board but not the rear transition module.

Note – Slots 1 through 6 and 9 through 14 are available for Netra CP3020 boards. Slots 7 and 8 are reserved for the CP3140 switch card.

2.5.1 Installing a Rear Transition Module

A compatible rear transition module must be used with the Netra CP3020 board for rear I/O access. The rear transition module enables access to the network, a boot device, and a console terminal. You can use the Netra CP30X0 rear transition module or you can design your own transition module.

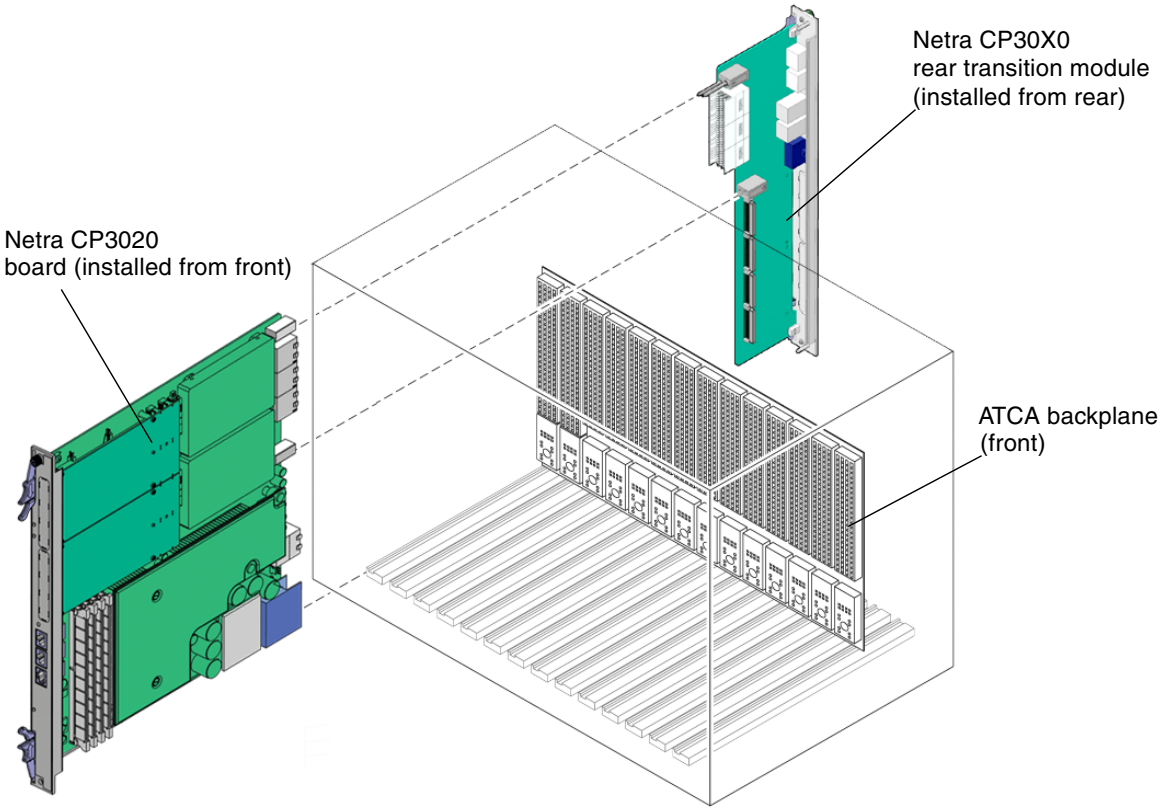


FIGURE 2-12 Installing the Netra CP30X0 Rear Transition Module

To install a rear transition module, follow these steps:

1. **Verify that you have taken the necessary antistatic precautions.**
2. **From the rear of the system, choose an appropriate slot for the rear transition module.**

   If you are installing a rear transition module, you must install it inline behind the accompanying Netra CP3020 board. For example, if the Netra CP3020 board will be installed in slot 3, the corresponding rear transition module must be installed at the back of the system in slot 3 (FIGURE 2-12). If you do not install the rear transition module and the Netra CP3020 board in corresponding slots, the system will recognize the Netra CP3020 board, but not the rear transition module.

Note – Slots 1 through 6 and 9 through 14 are available for Netra CP3020 boards. Slots 7 and 8 are reserved for the CP3140 switch card.

---

3. **Remove the slot filler panel from the selected slot, if necessary.**
4. **Retrieve the rear transition module from the ship kit.**
5. **Perform any PIM card installation or configuration procedures, if necessary.**

   Refer to the documentation that you received with the **PIM card** and to the *Netra CP30X0 Board User's Guide* for more information.

6. **Prepare the rear transition module by opening the injector/ejector latches at the top and bottom of the module (**FIGURE 2-13**).**

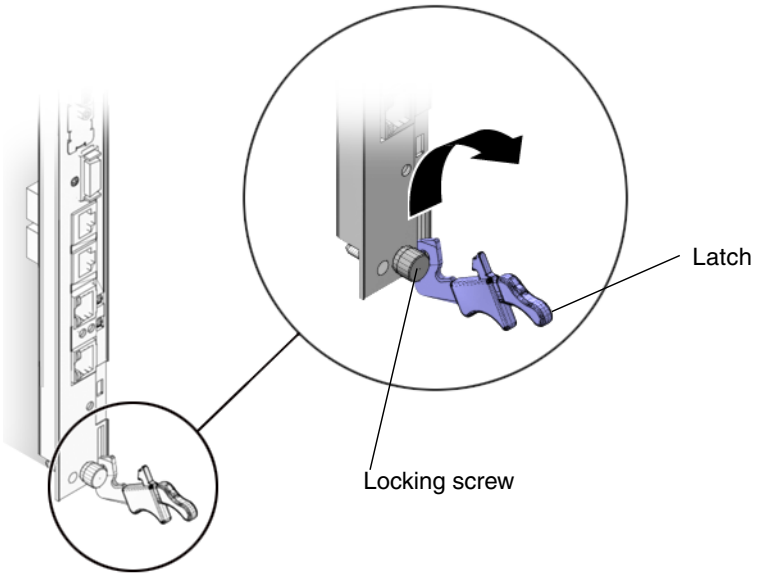


FIGURE 2-13 Injector/Ejector Latch and Locking Screw on the Rear Transition Module

7. **Carefully align the edges of the rear transition module with the card guides in the appropriate slot.**

   Look into the enclosure to verify correct alignment of the rails in the guides.

8. **Keep the rear transition module aligned in the guides, and slide the rear transition module in until the injector/ejector latches engage the card cage.**

9. **Push the rear transition module into the backplane connectors, and close the latches.**

10. **Tighten the locking screws to ensure that the module is secured into the ATCA shelf.**

11. **Install the Netra CP3020 board into the front of the ATCA shelf in the corresponding slot.**

    See "Installing the Netra CP3020 Board" on page 2-25 for instructions.

2.5.2 Installing the Netra CP3020 Board

Note – You can install the Netra CP3020 board in any available slot in the ATCA shelf except for slots 7 and 8.

To install the Netra CP3020 board, follow these steps:

1. **If you have installed a rear transition module, go to the front of the system and locate the same slot number where you installed the rear transition module.**
2. **Remove the filler panel from the board slot, if necessary.**

   The filler panel is secured to the card cage using two screws, one at the top of the filler panel, the other at the bottom. Store the filler panel in a safe place; you might need to use it again if you remove a board for an extended time.
3. **Prepare the Netra CP3020 board by opening the injector/ejector latches (**FIGURE 2-14**).**

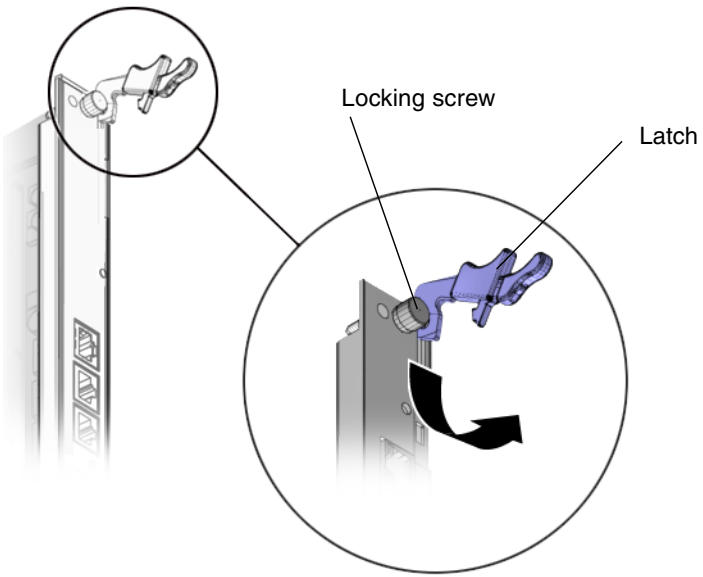


FIGURE 2-14 Injector/Ejector Latch and Locking Screw on the Netra CP3020 Board

4. **Carefully align the edges of the board with the guides in the appropriate slot.**

   Look into the enclosure to verify correct alignment of the rails in the guides.

5. **Keep the board aligned in the guides and slide the board in until the injector/ejector latches engage the card cage.**

6. **Push the board slightly into the backplane connectors and close the latches to seat the board in the connectors.**

   When the lower latch is closed, the blue Hot-Swap LED blinks (FIGURE 2-15) while the board is initializing. The blue LED turns off and the green OK LED lights when the board is ready for use.

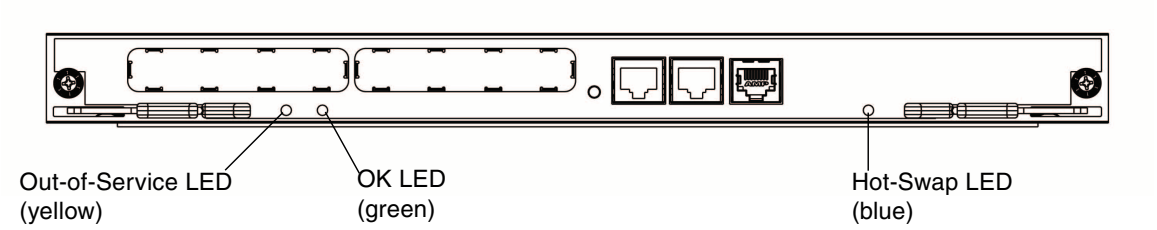


FIGURE 2-15 LEDs on the Netra CP3020 Board

7. **Tighten the locking screws and the top and the bottom of the Netra CP3020 board to ensure that it is secured to the ATCA shelf (FIGURE 2-13).**

2.6 Connecting External I/O Cables

Front panel ports are typically used for maintenance and troubleshooting purposes in installed and running systems. External I/O cables are connected to the Netra CP3020 board or to the Netra CP30X0 rear transition module when a rear transition module is used.

Note – Use shielded cables for Ethernet ports on the rear transition module. Ensure that the shield is grounded at both ends.

To connect each of these following cables:

- For Ethernet connections, Category 5e or better network cable is required. One end of the Ethernet cable is connected to a suitable 10/100/1000-Mbit Ethernet switch and the other end to one of the Ethernet ports on the Netra CP3020 board or Netra CP30X0 rear transition module. Both Ethernet port A (device `amd8111s0`) and Ethernet port B (device `bge4`) are available. By default, when a Netra CP30X0 rear transition module is installed, the Ethernet cables are

connected only to the Ethernet ports on the rear transition module. Refer to the *Netra CP30X0 Rear Transition Module User's Guide* (819-1187) for more information.

Note – Although the front panel Ethernet ports do not support Gigabit Ethernet, they can be connected to a Gigabit switch capable of 10/100/1000-Mbit Ethernet.

- Asynchronous serial I/O cables are attached from serial communication devices to the RJ-45 serial ports on the CP3020 board or CP30X0 rear transition module. If you are using serial port A on the CP3020 board, do not use serial port A on the CP30X0 rear transition module.

2.6.1 Connecting Cables for a System Console Running the Solaris Operating System

1. **Connect a serial cable to the serial console port on the front panel of the Netra CP3020 board (FIGURE 2-16) or the Netra CP30X0 rear transition module.**
2. **Connect the other end of the serial cable to the serial port of the system serving as the serial console.**

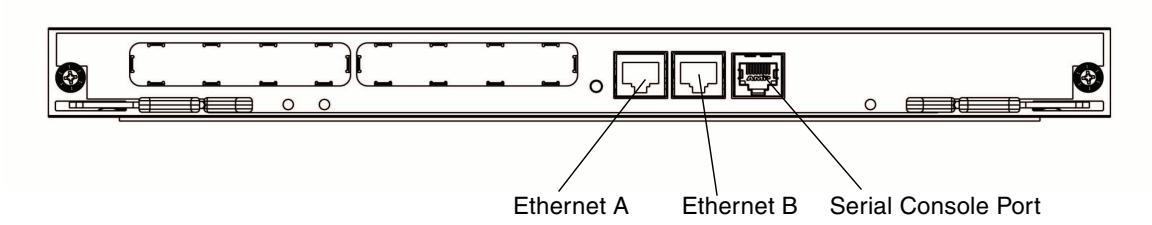


FIGURE 2-16 Front Connectors on the Netra CP3020 Board

3. **Use one of the following to establish a full-duplex serial terminal connection with the Netra CP3020 board:**
   - The `tip` utility
   - The `minicom` utility
   - A `telnet` utility (Connect to the proper port on a Network Terminal Server to which the Netra CP3020 is connected.)
   - Another suitable serial communications program on the system console

   For example, if you are using a UNIX system as the system console, at the UNIX prompt in a command tool or shell tool, type the following:

   For serial port A, type:

```
# tip -9600 /dev/ttya
```

For serial port B, type:

```
# tip -9600 /dev/ttyb
```

2.6.2 Connecting Cables to the System Console

1. **Connect a serial cable to the serial console port on the front panel of the Netra CP3020 board (FIGURE 2-16) or the Netra CP30X0 rear transition module.**
2. **Connect the other end of the serial cable to the serial port of the system serving as the system console.**
3. **Set the serial communications settings to 9600 baud, 8 bit, 1 stop bit, and no parity.**

2.6.3 SAS Port

The SAS port on the Netra CP3020 board or Netra CP30X0 rear transition module requires an external 4X SAS cable. The other end of the 4X SAS cable is typically connected to a storage device. Separate external 4X SAS cables can be attached to the Netra CP3020 SAS port and the Netra CP30X0 SAS port at the same time.

2.6.4 PMC I/O Cables

For optional PMC I/O cables, such as a printer cable, connect the cables according to the manufacturer's specifications.

CHAPTER 3

Software Configuration

This chapter describes the operating systems supported by the Netra CP3020 board. It also contains information about hot-swap capabilities and installing SunVTS™ software.

This chapter contains the following sections:

3.1 Operating Systems

The Netra CP3020 board supports the following operating systems:

- MontaVista Carrier Grade Linux version 3.1
- Solaris 10 OS, Release S10U1 and subsequent versions that may be tested for compatibility with the Netra CP3020 board. See the *Netra CP3020 Board Product Notes* (819-1181) for information on the Netra patches.

For information on the MontaVista Carrier Grade Linux operating system, see the documentation that came with the MontaVista operating system.

For information on versions of the Solaris Operating System, including installation, see the appropriate Solaris Documentation Collection at the Sun Documentation web site at:

http://www.sun.com/documentation/

3.2 Hot-Swapping the Netra CP3020 Board

The Netra CP3020 board supports hot-swapping and includes a blue Hot-Swap LED.

- **From the system console, shut down the operating system.**

  When the operating system is shut down, you can safely remove the board. Pull out the lower ejection handle (FIGURE 4-1) and wait for the blue Hot-Swap LED to light steadily before removing the board.

3.3 Downloading and Installing SunVTS

Note – The Sun Validation Test Suite (SunVTS software) runs on the Solaris Operating System only. There are similar test suites available for Linux operating systems.

The SunVTS software is a comprehensive software suite that tests and validates the Netra CP3020 board by verifying the configuration and function of most hardware controllers and devices on the board.

SunVTS software is used to validate a system during development, production, inspection, troubleshooting, periodic maintenance, and system or subsystem stressing. SunVTS software can be tailored to run on various types of machines, ranging from desktops to servers with modifiable test instances and processor affinity features.

You can perform high-level system testing by using the appropriate version of SunVTS software. For detailed information on SunVTS software support and downloads, refer to the following web site:

```
http://www.sun.com/oem/products/vts/
```

You will be prompted for your Sun Online Account name and password.

Ensure that the SunVTS software version is compatible with the Solaris Operating System being used. Information on the version of the SunVTS software installed on the Netra CP3020 board can be found in the file:

```
/opt/SUNWvts/bin/.version
```

To obtain SunVTS documentation, contact your local Customer Service representative, field applications engineer, or system support engineer.

Note – For security reasons, only a superuser is permitted to run SunVTS software. Installation and starting instructions are included with the software when it is downloaded.

CHAPTER 4

Powering On and Configuring BIOS Settings

This section describes how to power on and power off the Netra CP3020 board and how to use the BIOS to configure the board.

This chapter contains the following procedures and information:

Note – Netra CP3020 boards are powered on via the H8 BMC. When you install the board into a slot in the ATCA shelf, the board sequences through power-on states until it is fully powered on.

4.1 Performing a Reset on the Netra CP3020 Board

Note – Before powering on the Netra CP3020 board for the first time, follow the installation and cabling instructions in Chapter 2.

Caution – Do not operate the ATCA shelf without all fans, component heatsinks, air baffles, and covers installed. Severe damage to components can occur if the ATCA shelf is operated without adequate cooling mechanisms.

1. **Use a ballpoint pen or other stylus to press and release the recessed Reset button on the front of the Netra CP3020 board (FIGURE 4-1).**
2. **Confirm the progress of the reset by monitoring the BIOS POST messages.**

   When the board initializes, the green OK LED lights steadily.

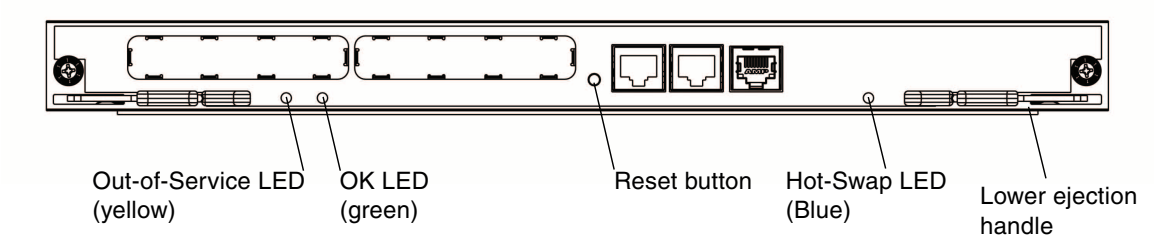


FIGURE 4-1 Netra CP3020 Board Front Panel

4.2 Powering Off the Netra CP3020 Board

1. **Choose a method for shutting down the Netra CP3020 board from main power mode to standby power mode:**
   - Graceful shutdown – Log in to the system and shut down the operating system using the appropriate operating system commands. Then pull out the lower ejection handle (FIGURE 4-1) and wait for the blue Hot-Swap LED to light steadily before removing the board.

- Emergency shutdown – Pull out the lower ejection handle and wait for the blue Hot-Swap LED to light steadily.

Note – The emergency shutdown procedure does not wait for the operating system to shut down cleanly. There is a potential for data loss.

4.3 Automatic Power-Off Events

A power-off sequence is initiated either by a request from the shelf manager or a fault condition. The Netra CP3020 board shuts down to standby power mode.

The following conditions trigger the shelf manager to issue a shutdown request:

- An overtemperature condition for more than one second
- Multiple fan failures

The following fault conditions trigger a shutdown:

- All power supplies have failed or have been removed.
- A power supply has been operating outside of predefined limits for more than 100 ms.
- The hot-swap circuit has faulted.
- An overtemperature condition has occurred.

4.4 Configuring BIOS Settings

This section describes how to view and modify the BIOS settings.

The BIOS has a Setup utility stored in the BIOS flash memory. The Setup utility reports system information and can be used to configure the BIOS settings. The configured data is provided with context-sensitive help and is stored in the system's battery-backed CMOS RAM. If the configuration stored in the CMOS RAM is invalid, the BIOS settings will default to the original state specified at the factory.

The BIOS Setup utility contains seven menu screens, which are displayed in this order: Main, Advanced, PCI/PnP, Boot, Security, Chipset, and Exit. See Appendix B for a BIOS menu tree and illustrations of the screens.

Use the left and right arrow keys to move sequentially through the seven screens. Fields that can be reconfigured are displayed in color. All other fields are non-configurable. Use the up and down arrow keys to scroll through a screen's menu. Use the Tab key to move across columns.

4.4.1 Changing the Configuration of a BIOS Menu Item

You can change the BIOS configuration by using a terminal (or terminal emulator connected to a computer) through the serial console port on the front of the Netra CP3020 board.

Note – Using the ANSI terminal emulation mode provides the best viewing of the BIOS screens.

---

1. **To change the system's parameters, enter the BIOS Setup utility by pressing the F2 key while the system is performing the power-on self-test (POST).**

   Refer to TABLE 4-1 for summary descriptions of the BIOS screens.

   The first BIOS Setup menu screen is displayed.

2. **Highlight the field to be modified using the arrow and Tab keys.**

3. **Press Enter to select the field.**

   A dialog box is displayed. The box presents you with the options available for the setup field that you have chosen.

4. **Modify the setup field and close the screen.**

5. **To modify other setup parameters, use the arrow and Tab keys to navigate to the appropriate screen and menu item, repeat Step 2 through Step 4. Otherwise, go to Step 6.**

6. **Press and release the right arrow key until the Exit menu screen is displayed.**

7. **Follow the instructions on the Exit menu screen to save your changes and exit the Setup utility.**

4.4.2 BIOS Considerations

This section contains special considerations regarding the system BIOS.

4.4.2.1 Serial Attached SCSI (SAS) Devices

The Netra CP3020 LSI 1064 SAS device supports up to four SAS devices. Two of these device ports are used to support the two SAS drives, ID 0 and ID 1. Both of these drives are located the Netra CP3020 board itself. The Netra CP3020 board also supports SAS drive ID 2 and ID 3 via the rear transition module.

4.4.2.2 BIOS Option ROMs on the Netra CP3020 Board

The Netra CP3020 board has an option ROM for each of the following components:

- LSI 1064 SAS controller
- Broadcom BCM 5704C base interface
- Broadcom BCM 5704S fabric interface
- Broadcom BCM 5705F administration interface
- AMD 8111 Ethernet administration interface

4.4.2.3 AMD PowerNow! Feature Disabled by Default

The AMD PowerNow! feature, which is accessed from the BIOS Setup utility Advanced menu, is disabled by default on the Netra CP3020 board. Some problems have been observed when using this feature on certain operating systems. If you want to enable this feature, first refer to the *Netra CP3020 Board Product Notes* (816-4961) for any outstanding known issues for your operating system.

4.4.3 Description of the BIOS Screens

TABLE 4-1 contains summary descriptions of the first-level BIOS Setup screens. For more information about the BIOS screens and screen illustrations, see Appendix B.

TABLE 4-1 BIOS Setup Screens Summary

Screen	Description
Main	General system information.
Advanced	Configuration information for the CPUs, IDE, SuperI/O, ACPI, Event Log, HyperTransport, IPMI, MPS, Remote Access, and USB. Twelve separate screens can be accessed from the Advanced menu.
PCI/PnP	Configure Plug-and-Play (PnP) devices. Note: For some operating systems you can also configure PnP devices via the operating system.
Boot	Configure the boot device priority (hard disk drives and the ATAPI DVD-ROM drive).
Security	Install or change the user and supervisor passwords.
Chipset	Configuration options for the NorthBridge, SouthBridge, and PCI-X devices. Six separate screens can be accessed from the Chipset menu. Note that the Memory Chipkill option is enabled by default. Enabling Chipkill improves system reliability but degrades system performance under specific applications.
Exit	Save or discard changes.

4.5 Setting Supervisor and User Passwords

You must set the Supervisor password before you can set the User password. The Supervisor password sets the desired access level for the User password. The Clear CMOS jumper clears any BIOS passwords you have set. See Section 4.7, “Clearing CMOS Settings” on page 4-11 for further details.

4.6 Setting the Boot Device Using BIOS Setup Screens

Before beginning this procedure, ensure that you have installed the serial cable as described in Section 2.6, "Connecting External I/O Cables" on page 2-26.

Note – See Section 4.4.3, "Description of the BIOS Screens" on page 4-6 for descriptions of the first-level BIOS menu screens. See Appendix B for a BIOS menu tree and illustrations of the first-level and second-level BIOS screens.

---

1. **Use terminal emulation software to configure the serial COM1 settings. Use the ANSI terminal type setting.**
2. **Set the serial communication settings to 9600 baud, 8 bit, 1 stop bit, no parity.**
3. **Power on the ATCA shelf.**

   The BIOS starts running POST.
4. **Press the `F2` key to interrupt the boot and access the BIOS Main menu (FIGURE 4-2).**

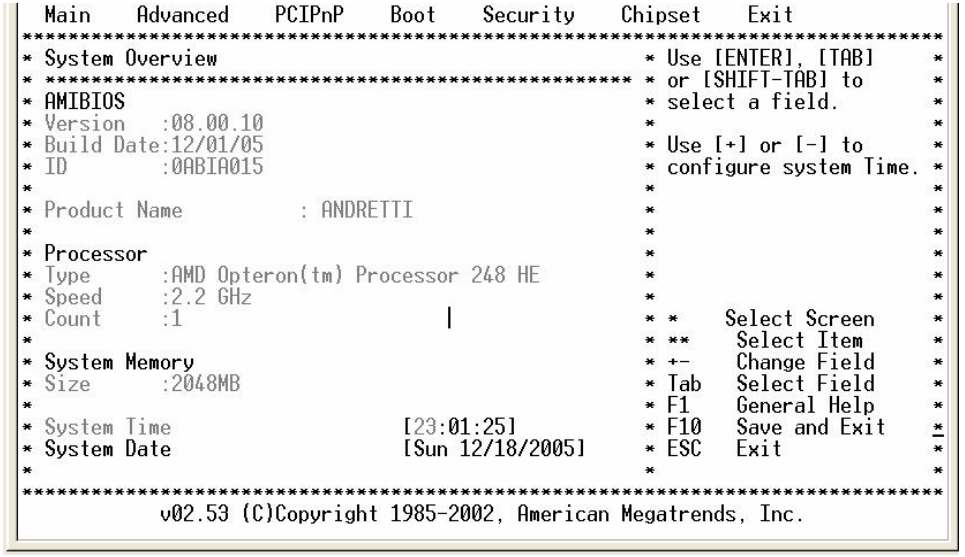


FIGURE 4-2 BIOS Main Menu

5. **Using the arrow keys, move across the top of the screen to the Boot menu and press the Enter key.**

   The Boot Settings menu is displayed (FIGURE 4-3).

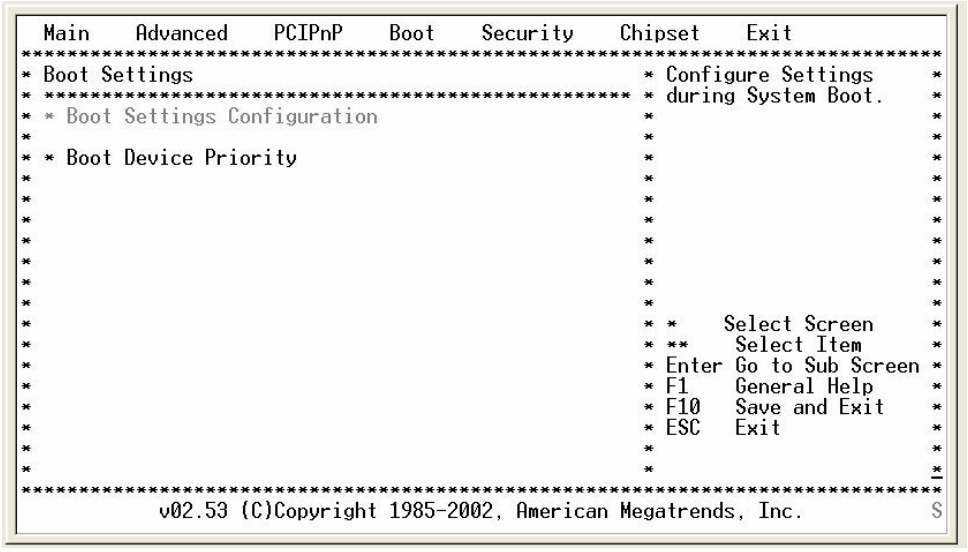


FIGURE 4-3 Boot Settings Menu

6. **Move down the list, select the Boot Device Priority option, and press Enter.**

   The Boot Device Priority menu is displayed (FIGURE 4-4).

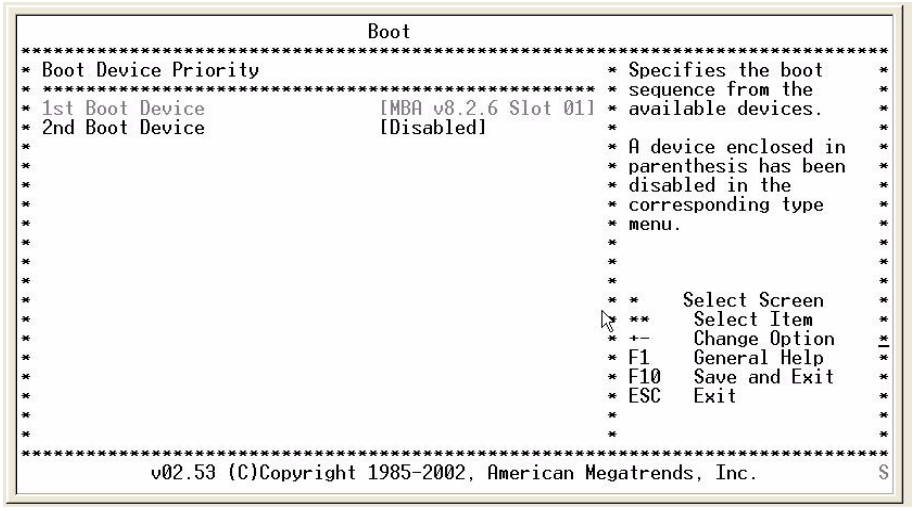


FIGURE 4-4 Boot Device Priority Menu

7. **Select the** `#210 ID01 LUN0 SEA` **device as the 1st Boot Device.**
8. **Disable all unneeded boot devices so that the menu appears like** FIGURE 4-5**.**

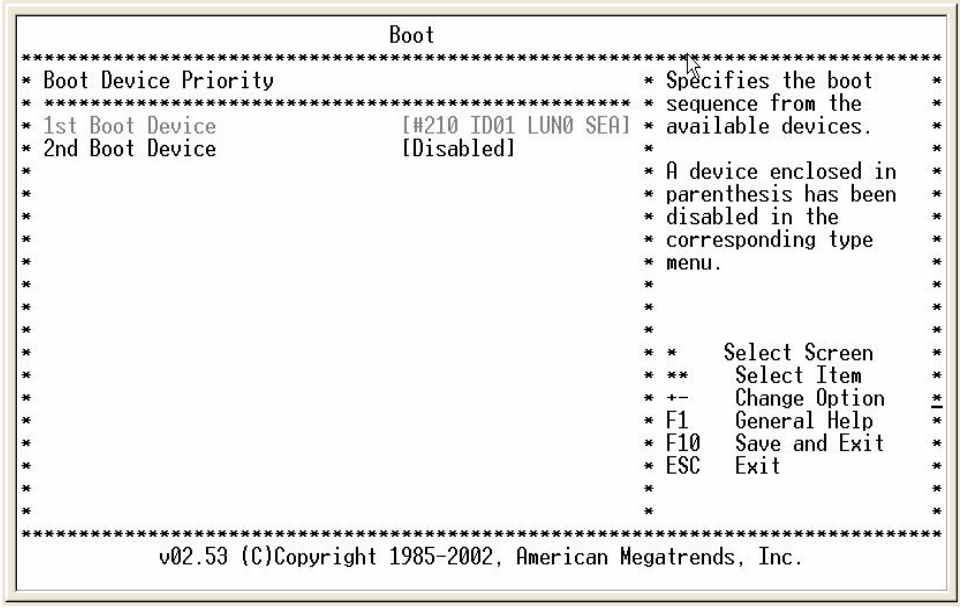


FIGURE 4-5 Completed Boot Device Priority Menu

9. **Use the arrow keys to move to the Exit menu, and press Enter.**

   The confirmation dialog box is displayed.

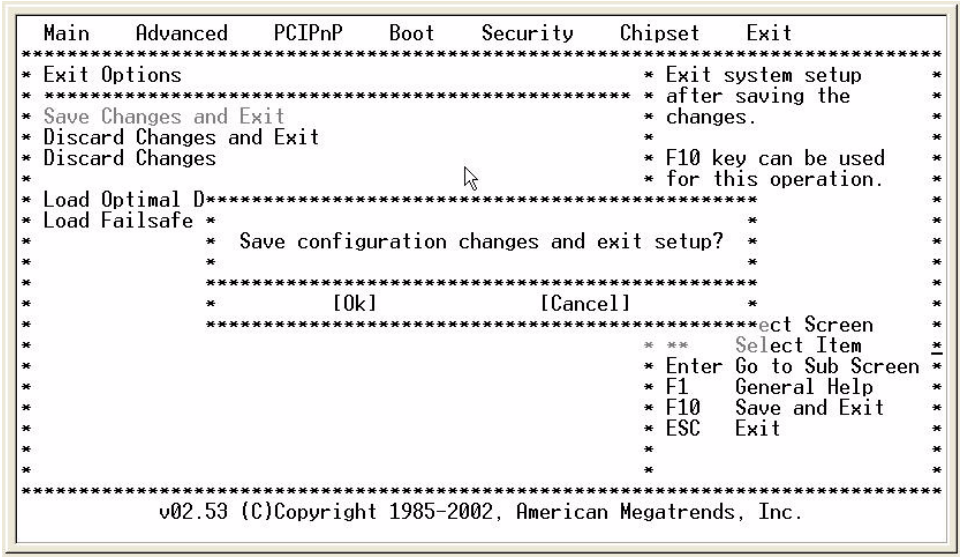


FIGURE 4-6 Confirmation Dialog Box

10. **Press Enter to select Ok.**

    The BIOS boots the selected device. The operating system on the selected boot device loads.

11. **Configure the operating system by providing a locale, system name, IP address, and other information.**

    Refer to the documentation for your operating system for information on configuring the operating system.

4.7 Clearing CMOS Settings

You can use jumper 3 to clear the CMOS settings. For example, if you inadvertently set the console BAUD rate to a rate that your system console cannot support, use this jumper to invalidate the settings and reboot with defaults. This procedure also resets the Supervisor and the User passwords.

Jumper 3 is located on the Netra CP3020 board between the Compact Flash socket and four capacitors (FIGURE 4-7).

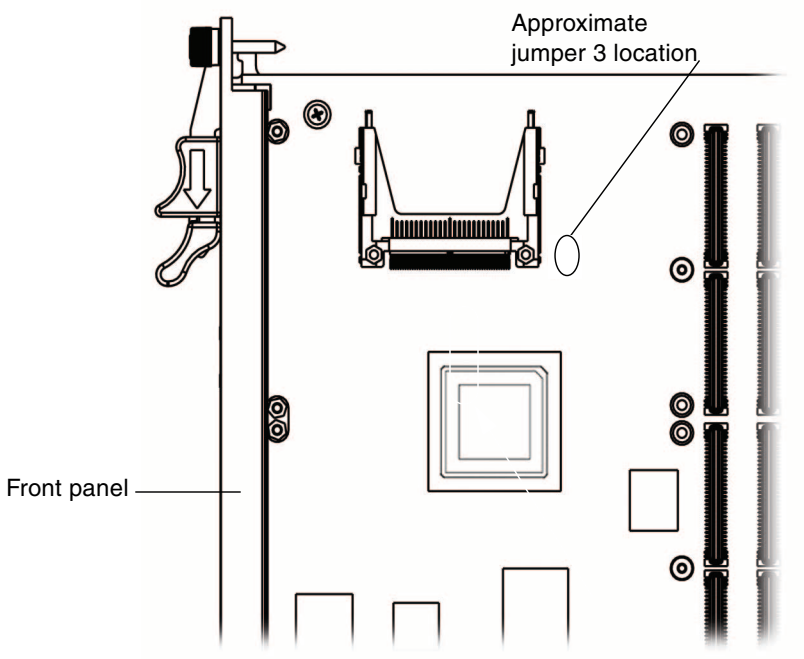


FIGURE 4-7 Jumper 3 Location

4.7.1 Removing the Netra CP3020 Board

You must remove the Netra CP3020 board before you can reset the jumper.

1. **Gracefully shut down the Netra CP3020 board.**

   Use the instructions in Section 4.2, "Powering Off the Netra CP3020 Board" on page 4-2.

   The blue Hot-Swap LED blinks and then lights steadily when it is safe to remove the board.

2. **If installed, remove all cables from the front of the Netra CP3020 board.**
3. **Loosen the locking screws to release the board from the ATCA shelf.**
4. **Release the upper latch first and then the lower latch to unseat the board from the connectors.**
5. **Remove the board from the ATCA shelf and place the board on an antistatic mat.**

4.7.2 Resetting Jumper 3

Jumper 3 is shown in FIGURE 4-7 and FIGURE 4-8. The jumper housing should be stored in the P1/P2 position, which is the run position.

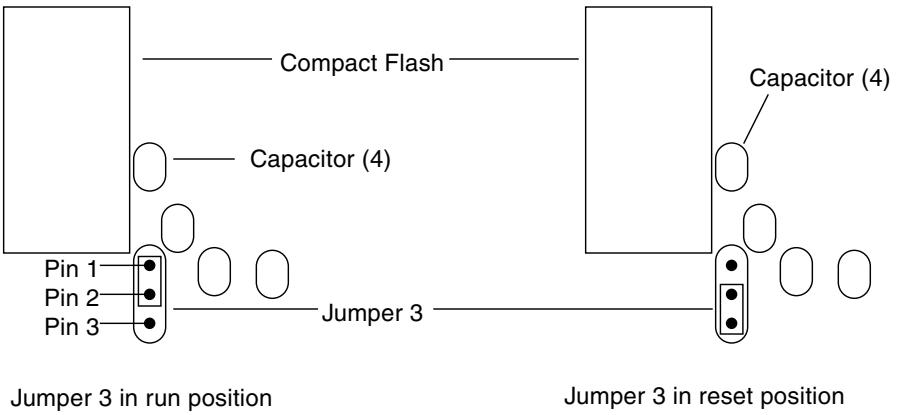


FIGURE 4-8 Jumper 3 in the Run and Reset Positions

TABLE 4-2 provides information on the pin functions on jumper 3.

TABLE 4-2 Pin Functions on Jumper 3

Pin Number	Purpose
Pin 1	Battery Feed
Pin 2	VCC_RTC (destination for battery power)
Pin 3	BATT_CLR (resistor to GND, used to drain capacitive charge and clear the CMOS memory)

To reset the jumper and return the CMOS settings to the default settings, perform the following steps:

1. **Remove the jumper housing from the run position (P1/P2) and move it to the reset position (P2/P3).**
2. **Wait at least five seconds for the CMOS settings to reset and then move the jumper housing back to the run position.**

3. **Reinstall the board.**

   Use the procedure in Section 2.5.2, "Installing the Netra CP3020 Board" on page 2-25.

Note – The board will operate normally only when the jumper housing is in the run position.

---

4. **Press the `F2` key to interrupt the boot and access the BIOS Main menu (FIGURE 4-2).**
5. **Press and release the right arrow key until the Exit menu is selected. Press the Enter key.**
6. **Select the Load Optimal Defaults option and press the Enter key.**
7. **Use the arrow keys to return to the BIOS Main Menu.**
8. **Use the arrow keys to move down the main menu and reset the System Time and System Date fields.**
9. **Use the arrow keys to move to the Exit Menu.**
10. **Choose Save Changes and Exit.**
11. **Select OK to confirm the changes you made.**

4.8 Updating the BIOS

When they become necessary, updated BIOS images will be available as patches on the following web site:

`http://sunsolve.sun.com/`

4.9 Power-On Self-Test

For information about BIOS POST testing, POST codes, POST code checkpoints, and console redirection, see Appendix C.

CHAPTER 5

Hardware Architecture

This chapter describes the hardware architecture of the Netra CP3020 board.

TABLE 5-1 describes the architecture and functions of the Netra CP3020 hardware.

TABLE 5-1 Netra CP3020 Hardware Architecture and Functions

Component	Function/Characteristics
Netra CP3020 board	• An ATCA node board based on an AMD Opteron processor, hot-swappable to an ATCA shelf. • Supports both single-core and dual-core processors. • Supports two Gigabit Ethernet interfaces as Base Fabric interfaces and two Gigabit SERDES interfaces as Extended Fabric interfaces to support redundant Dual Star topology. • Supports four VLP DDR-1 DIMMs, which can support the maximum memory of 8 Gbytes (maximum of 4 Gbytes for single CPU configurations). • Supports two PMC cards for PCI expansion.
I/O subsystem architecture: AMD 8132 ASIC	• Bridges between the Hypertransport and the PCI buses. • Provides a Hypertransport tunnel to the AMD 8111 ASIC. • Provides two PCI-X leafs to which the PMCs, Base Fabric, Extended Fabric, and SAS controller are connected.

TABLE 5-1 Netra CP3020 Hardware Architecture and Functions *(Continued)*

Component	Function/Characteristics
I/O controller: AMD 8111 ASIC	• Provides a built-in IDE controller. • Supports the Compact Flash interface. • SuperI/O connected to the 8111 PCI bus provides an RS-232 serial port, which is used for console access and available through the front and rear panels.
Connections	• SuperI/O provides a serial port used to interface with the H8 IMPI controller, which requires a serial connection to communicate with the AMD Opteron host CPU. • Pigeon Point H8 controller monitors all critical functions of the board, responds to commands from the shelf manager, and reports events. • Southbridge chip provides serial port routing to the H8 controller and the Base Fabric Ethernet controller for the Netconsole function. • BIOS boot flash interfaced to the AMD 8111 ASIC.
Power	• ATCA backplane provides redundant -48V power connections. • Netra CP3020 board derives the required power by using on-board DC/DC converters. • Standby power is generated separately from -48V and is provided for hardware management circuitry.

APPENDIX **A**

Physical Characteristics

Specifications for the Netra CP3020 board are provided in the following sections:

A.1 Form Factor

The Netra CP3020 board is a standard 8 rack unit (8U) factor, single-slot wide. It complies with the board mechanical dimensions that are required by the PICMG 3.0 R1.0 specification:

- 322.25 mm x 280 mm (12.7 inches x 11.0 inches)
- 30.48 mm (1.2 inch) front panel

A.2 Thermal Management

The heatsink was designed specifically for the Netra CP3020 board and is mechanically mounted to the board. The heatsink and DIMMs are positioned on the board to provide adequate airflow (bottom to top).

Note – The default settings for MD2, MD1, NMI, and FWE set the H8 controller to Mode 2, User Programming Mode.

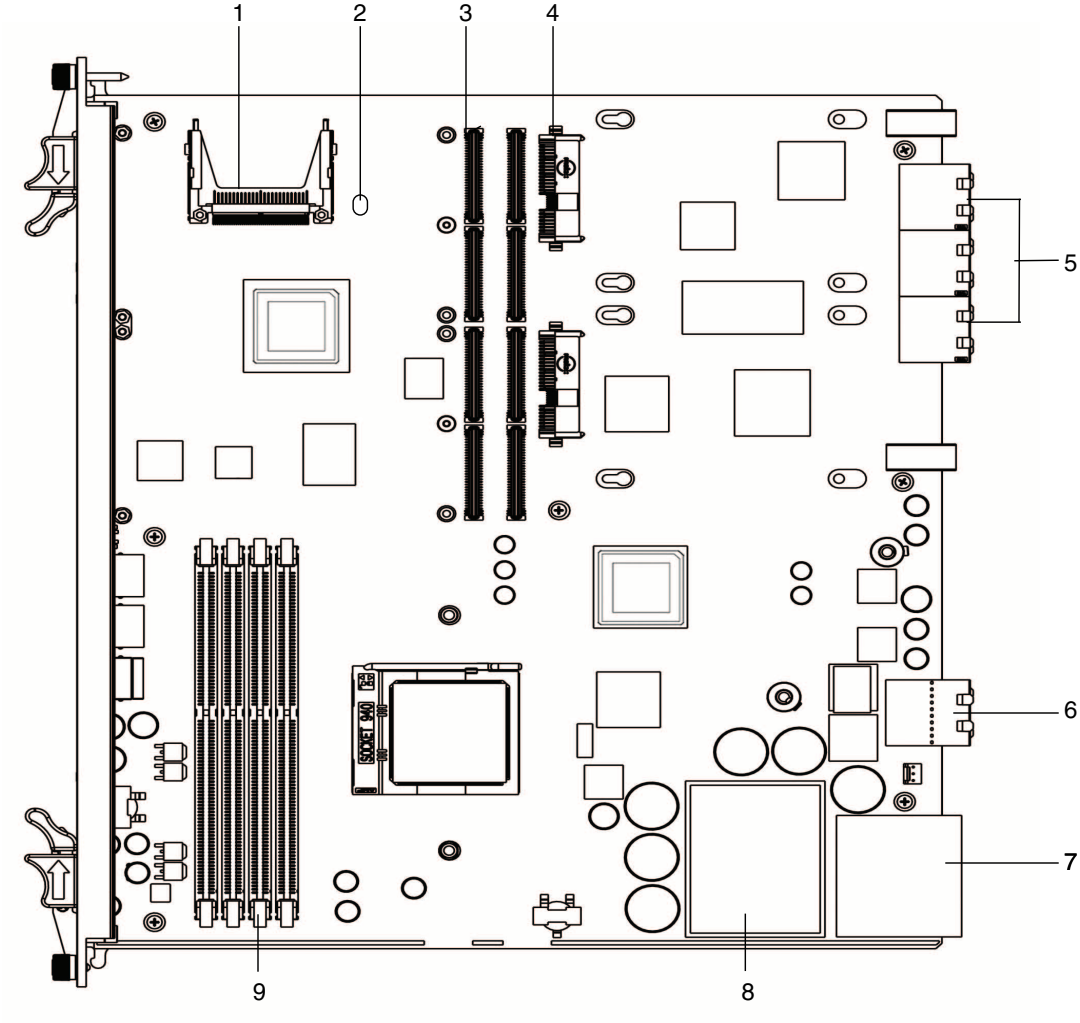
TABLE A-1 lists the jumper settings for thermal management.

TABLE A-1 Jumper Settings

Jumper	Open	Short Pin 1 to Pin 2	Short Pin 2 to Pin 3
J2601	Normal Operation [Default]	Force Power-On-Reset	Force `XIR` reset
J3301	Do Not Use	Normal Operation [Default]	Clear `Real_Time_Clock`
J3702	Write Protect `SUN FRUID` [Default]	Enable Write of `SUN FRUID`	N/A

A.3 Layout

The Netra CP3020 board layout is shown in FIGURE A-1.



1. Compact Flash connector
2. Jumper 3 location
3. PMC connectors
4. Disk drive connector
5. Zone 3 connector
6. Zone 2 connector
7. Zone 1 connector
8. Power module -48 to 12 V
9. DIMMs

FIGURE A-1 Netra CP3020 Board Layout

A.4 Connectors and Pinouts

A.4.1 Front Panel Connectors

The front panel has the following connectors:

- Two 10/100BASE-T Ethernet ports (RJ-45)
- One serial port (RJ-45)

A.4.1.1 Ethernet Ports

The Ethernet connectors are RJ-45 connectors. The controller auto-negotiates to either 10BASE-T or 100BASE-T. The pinouts in FIGURE A-2 and TABLE A-2 apply to both of the Ethernet ports.

FIGURE A-2 shows the Ethernet port connectors

.

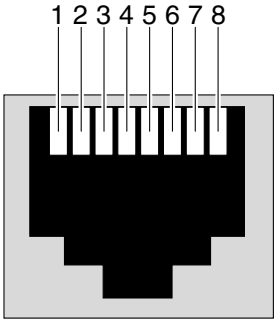


FIGURE A-2 Ethernet RJ-45 Connectors

TABLE A-2 proves the eight pin assignments for the Ethernet port connector.

TABLE A-2 Ethernet Port Connector Pin Assignments

Pin	Signal Name	Pin	Signal Name
1	TXD+	5	Not used

TABLE A-2 Ethernet Port Connector Pin Assignments *(Continued)*

Pin	Signal Name	Pin	Signal Name
2	TXD-	6	RXD-
3	RXD+	7	Not used
4	Not used	8	CTS

TABLE A-3 provides definitions for wire colors and pin numbers in the RJ-45 connector.

TABLE A-3 RJ-45 Wire Colors and Adapter Pins

Wire Colors	RJ-45 Pin Number
Blue	1
Orange	2
Black	3
Red	4
Green	5
Yellow	6
Brown	7
White	8

A.4.1.2 DB-9 Female Connector

TABLE A-4 provides functional descriptions of the pins in the DB-9 connector.

TABLE A-4 DB-9 Connector Pins

Function	Pin Number
Clear to send	8
Data carrier detect	1
Received data	2
Signal ground	5
Transmitted data	3
Data terminal ready	4

TABLE A-4 DB-9 Connector Pins *(Continued)*

Function	Pin Number
Request to send	7
Data set ready	6
Ring indicator	9

A.4.1.3 Signal Names and Pin Numbers in Various Ethernet Connectors

TABLE A-5 provides comparisons between various Ethernet connectors, pin positions, and signal names.

TABLE A-5 Pin Numbers and Signal Names in Various Ethernet Connectors

	Netra CP3020 Console to PC COM Port (DTE to DTE)	CAT 5e Cable	Straight Through	RJ-45 to DB-9 Female Adapter	
Signal Name	Netra CP3020 RJ-45 Female Pin #	Male RJ-45 Pin Number	Male RJ-45 Pin Number	Female RJ-45 Pin Number	DB-9 Female Pin Number
RTS -->	1	1	1	1 (blue)	8
DTR -->	2	2	2	2 (orange)	6
TxD -->	3	3	3	3 (black)	2
GND	4	4	4	4 (red)	5
GND	5	5	5	5 (green)	N/C
RxD <--	6	6	6	6 (yellow)	3
DSR <--	7	7	7	7 (brown)	4
CTS <--	8	8	8	8 (white)	7

A.4.1.4 Serial Port

FIGURE A-3 shows the connector pin assignments for the front panel serial port. TABLE A-6 lists the serial port connector pin assignments.

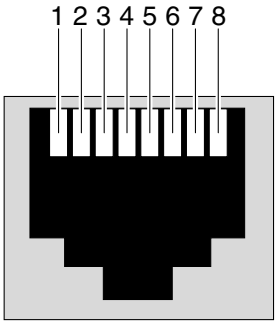


FIGURE A-3 Front Panel Serial Connectors

TABLE A-6 Serial Port Mini DIN 8-pin Connector Pinouts

Pin	Signal Name	Pin	Signal Name
1	RTS	5	DCD
2	DTR	6	RXD
3	TXD	7	DSR
4	GND	8	CTS

A.4.2 PMC Connectors

Four 64-pin connectors make up the PMC card connection. These connectors and pinouts are defined by the following industry-standard specifications:

- *Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC IEEE (MMSC) P1386.1/Draft 2.3*, October 9, 2000
- *Draft Standard for a Common Mezzanine Card Family: CMC IEEE (MMSC) P1386/Draft 2.3*, October 9, 2000

The PMC slots are available at the front panel. PMC I/O is taken through the rear transition module and is available using PIM.

A.4.3 Power Connector (Zone 1)

The Netra CP3020 board uses a 34-pin Positronic connector as the Zone 1 power distribution connector. It provides the support for the following signals:

- Two -48 VDC power feeds (four signals each; eight signals total)
- Two IPMB ports (two signals each; four signals total)
- Geographic address (eight signals)

The analog test and ring voltage pins are left unconnected. FIGURE A-4 shows the pin assignments.

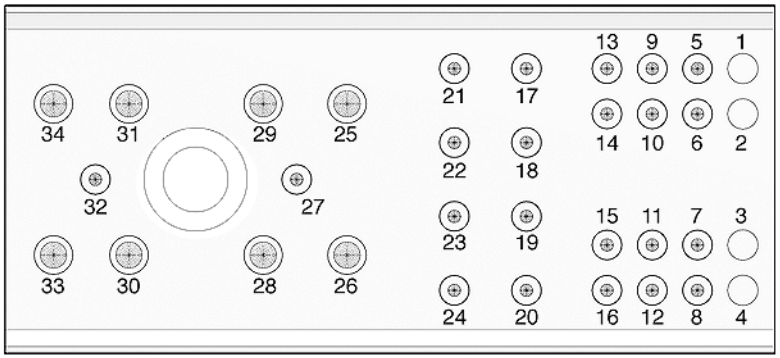


FIGURE A-4 Power Distribution Connector (Zone 1) P10

TABLE A-7 lists the power distribution connector pin assignments.

TABLE A-7 Power Distribution Connector Pin Assignments

Pin Number	Name	Description
1	Reserved	Reserved
2	Reserved	Reserved
3	Reserved	Reserved
4	Reserved	Reserved
5	HA0	HA0 Hardware Address Bit 0
6	HA1	HA1 Hardware Address Bit 1
7	HA2	HA2 Hardware Address Bit 2
8	HA3	HA3 Hardware Address Bit 3
9	HA4	HA4 Hardware Address Bit 4
10	HA5	HA5 Hardware Address Bit 5
11	HA6	HA6 Hardware Address Bit 6
12	HA7/P	HA7/P Hardware Address Bit 7 (Odd Parity Bit)
13	SCL_A	IPMB Clock, Port A
14	SDA_A	IPMB Data, Port A
15	SCL_B	IPMB Clock, Port B
16	SDA_B	IPMB Data, Port B

TABLE A-7 Power Distribution Connector Pin Assignments *(Continued)*

Pin Number	Name	Description
17	Unused	
18	Unused	
19	Unused	
20	Unused	
21	Unused	
22	Unused	
23	Unused	
24	Unused	
25	SHELF_GND	Shelf Ground
26	LOGIC_GND	Logic Ground
27	ENABLE_B	Enable B
28	VRTN_A	Voltage Return A
29	VRTN_B	Voltage Return B
30	EARLY_A	-48V Early A
31	EARLY_B	-48V Early B
32	ENABLE_A	Enable A
33	-48V_A	-48V A
34	-48V_B	-48V B

A.4.4 Data Transport Connector (Zone 2)

The data transport connector consists of one 120-pin HM-Zd connector, labeled P23, with 40 differential pairs. This is called the Zone 2 connector.

The Zone 2 connector provides the following signals:

- Two 10/100/1000BASE-T/TX Ethernet Base Fabric channels (four differential signal pairs each; 16 signals total)
- Two 2-Gbit SERDES ports on the Extended Fabric (two differential signal pairs each; eight signals total)

The connector vendor part number is Tyco: 1469001-1.

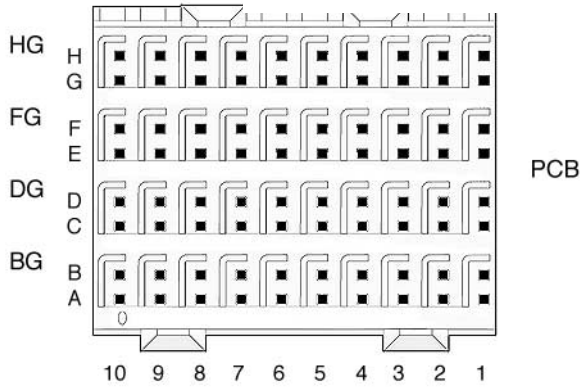


FIGURE A-5 Zone 2 Connector

A.4.5 Rear Transition Module Connector (Zone 3)

The Netra CP3020 board provides all the I/O connections for rear access through the Zone 3 rear transition module connector. The connector view and the pinout for the Zone 3 connector are shown in FIGURE A-6.

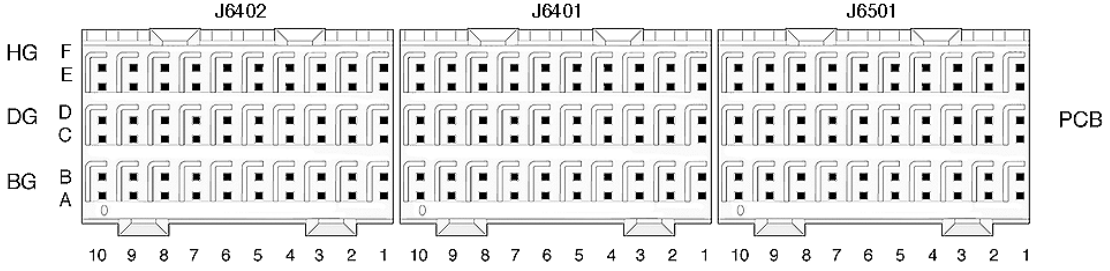


FIGURE A-6 Zone 3 Connector

TABLE A-8 shows the J6402 connector pin assignments.

TABLE A-8 J6402 Connector Pin Assignments

Row	A	B	BG	C	D	DG	E	F	FG
1	PMC1_IO1	PMC1_IO2		PMC1_IO3	PMC1_IO4		PMC1_IO5	PMC1_IO6	GND
2	PMC1_IO7	PMC1_IO8		PMC1_IO9	PMC1_IO10		PMC1_IO11	PMC1_IO12	
3	PMC1_IO13	PMC1_IO14		PMC1_IO15	PMC1_IO16		PMC1_IO17	PMC1_IO18	
4	PMC1_IO19	PMC1_IO20		PMC1_IO21	PMC1_IO22		PMC1_IO23	PMC1_IO24	
5	PMC1_IO25	PMC1_IO26		PMC1_IO27	PMC1_IO28		PMC1_IO29	PMC1_IO30	
6	PMC1_IO31	PMC1_IO32		PMC1_IO33	PMC1_IO34		PMC1_IO35	PMC1_IO36	GND
7	PMC1_IO37	PMC1_IO38		PMC1_IO39	PMC1_IO40		PMC1_IO41	PMC1_IO42	
8	PMC1_IO43	PMC1_IO44		PMC1_IO45	PMC1_IO46		PMC1_IO47	PMC1_IO48	
9	PMC1_IO49	PMC1_IO50		PMC1_IO51	PMC1_IO52		PMC1_IO53	PMC1_IO54	
10	PMC1_IO55	PMC1_IO56		PMC1_IO57	PMC1_IO58		PMC1_IO59	PMC1_IO60	

TABLE A-9 shows the J6401 connector pin assignments.

TABLE A-9 J6401 Connector Pin Assignments

Row	A	B	BG	C	D	DG	E	F	FG
1	PMC0_IO1	PMC0_IO2		PMC0_IO3	PMC0_IO4		PMC0_IO5	PMC0_IO6	GND
2	PMC0_IO7	PMC0_IO8		PMC0_IO9	PMC0_IO10		PMC0_IO11	PMC0_IO12	
3	PMC0_IO24	PMC0_IO23		PMC0_IO22	PMC0_IO21		PMC0_IO20	PMC0_IO19	
4	PMC0_IO18	PMC0_IO17		PMC0_IO16	PMC0_IO15	GND	PMC0_IO14	PMC0_IO13	
5	PMC0_IO36	PMC0_IO35	GND	PMC0_IO34	PMC0_IO33		PMC0_IO32	PMC0_IO31	
6	PMC0_IO30	PMC0_IO29		PMC0_IO28	PMC0_IO27		PMC0_IO26	PMC0_IO25	
7	PMC0_IO48	PMC0_IO47		PMC0_IO46	PMC0_IO45	GND	PMC0_IO44	PMC0_IO43	
8	PMC0_IO42	PMC0_IO41		PMC0_IO40	PMC0_IO39		PMC0_IO38	PMC0_IO37	
9	PMC0_IO49	PMC0_IO50		PMC0_IO51	PMC0_IO52		PMC0_IO53	PMC0_IO54	
10	PMC0_IO55	PMC0_IO56		PMC0_IO57	PMC0_IO58		PMC0_IO59	PMC0_IO60	

TABLE A-10 shows the J6501 connector pin assignments.

TABLE A-10 J6501 Connector Pin Assignments

Row	A	B	BG	C	D	DG	E	F	FG
1	PMC0_IO61	PMC1_IO2		PMC0_IO63	PMC0_IO64			-12V	GND
2	PMC1_IO61	PMC1_IO8	5V	PMC1_IO63	PMC1_IO64	5V	+12V	+12V	
3	RTM_SER1_CTS	PMC1_IO14	3.3V	RTM_SER1_DCD	RTM_SER1_DSR	3.3V	RTM_SER1_RXD	RTM_SER1_TXD	
4	RTM_SER1_RTS	PMC1_IO20	3.3V	RTM_SER2_CTS	RTM_SER2_DTR	3.3V	RTM_SER2_DCD	RTM_SER2_DSR	
5	RTM_SER2_RXD	PMC1_IO26	5V	RTM_SER2_RTS		5V			
6	RTM_HDD2_RX_P	PMC1_IO32	GND			GND	RTM_HDD2_TX_N	RTM_HDD2_TX_P	
7	RTM_PRSNT_N	PMC1_IO38	GND	SYS_I2C_SDA	SYS_I2C_SCL	GND	3V_STBY	3V_STBY	
8	RTM_HDD3_RX_P	PMC1_IO44	GND			GND	RTM_HDD3_TX_N	RTM_HDD3_TX_P	
9	RTM_TXD_1P	PMC1_IO50	GND	2.5V	2.5V	GND	RTM_RXD_1P	RTM_RXD_1N	
10	RTM_TXD_0P	PMC1_IO56	GND	2.5V	2.5V	GND	RTM_RXD_0P	RTM_RXD_0N	

APPENDIX **B**

BIOS Screens

This appendix provides examples of the first-level and second-level screens from the BIOS menu. To enter the BIOS menu, press the F2 key during the POST portion of the boot process.

FIGURE B-1 shows the BIOS menu tree. Figures B-2 through B-37 show the screens within the BIOS menu tree.

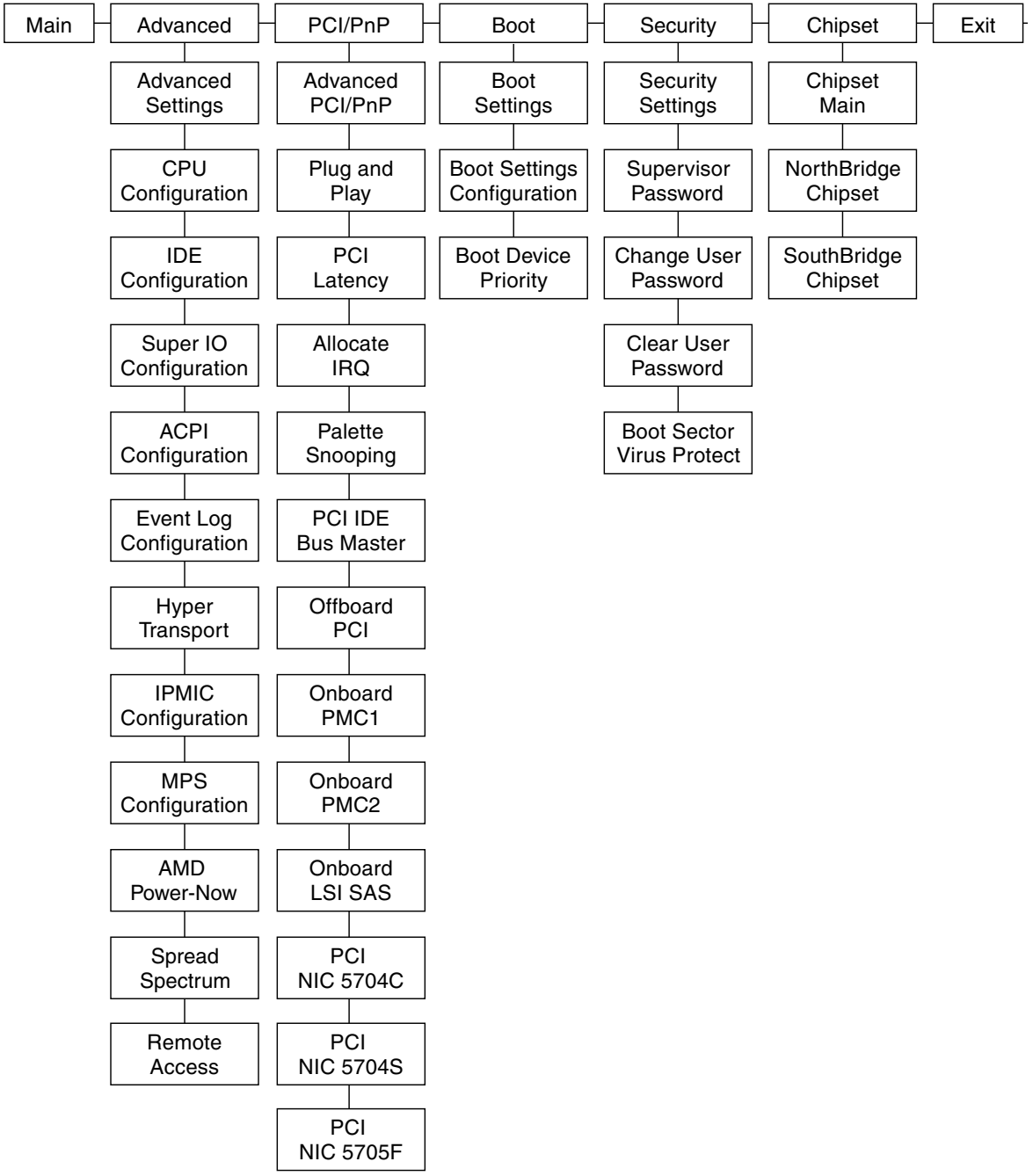


FIGURE B-1 BIOS Menu Tree

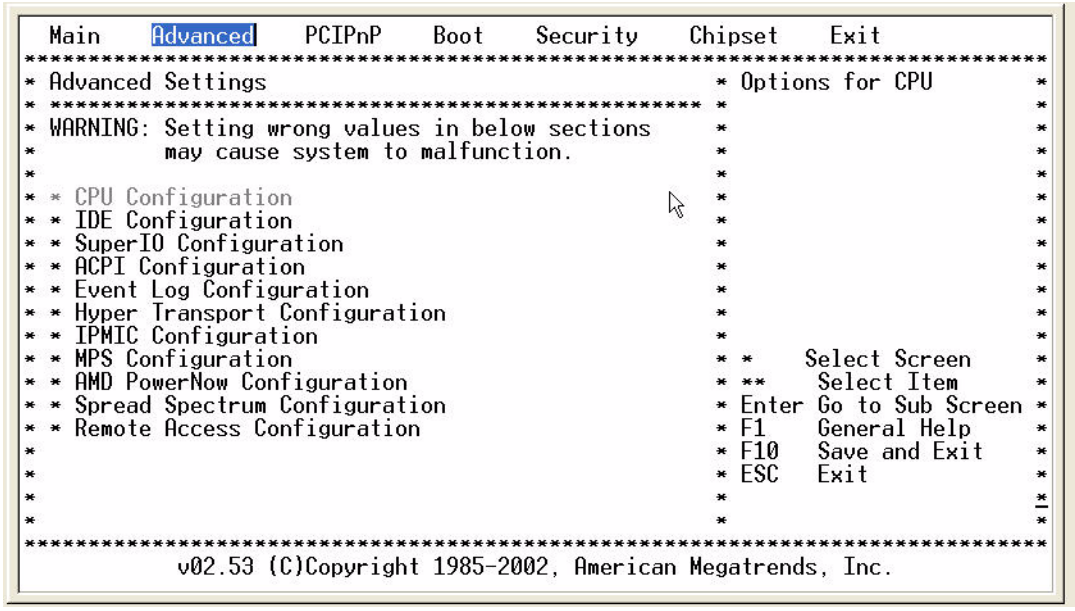


FIGURE B-2 Advanced Settings Menu

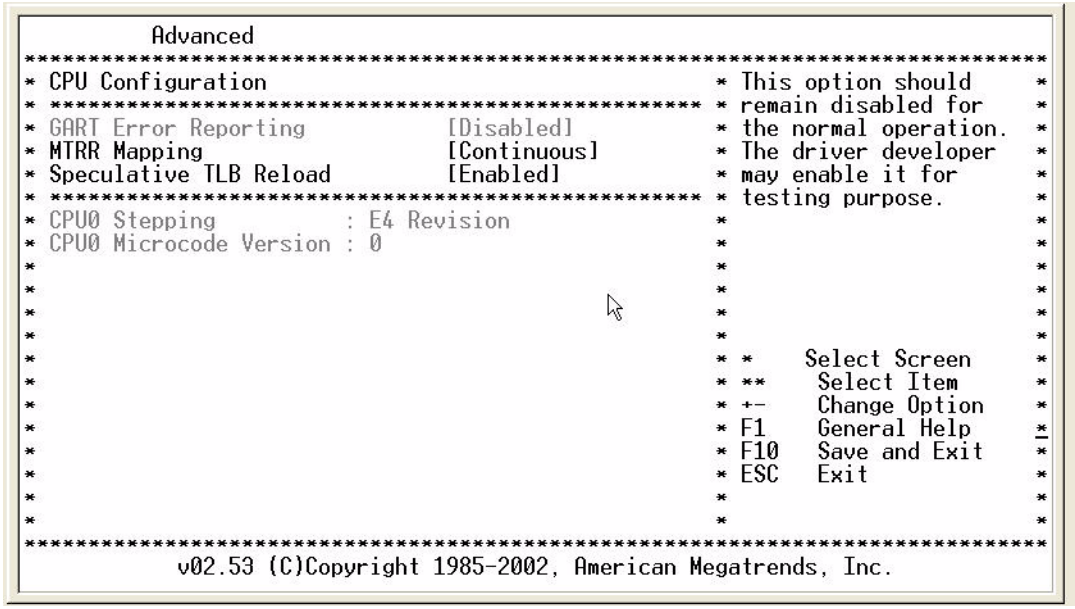


FIGURE B-3 CPU Configuration Menu

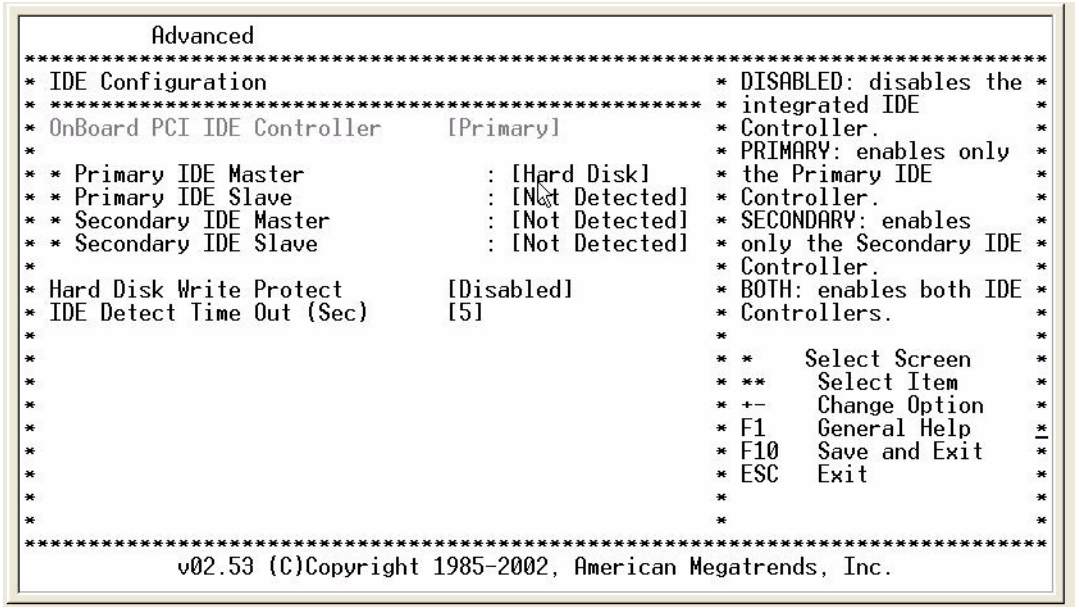


FIGURE B-4 IDE Configuration Menu

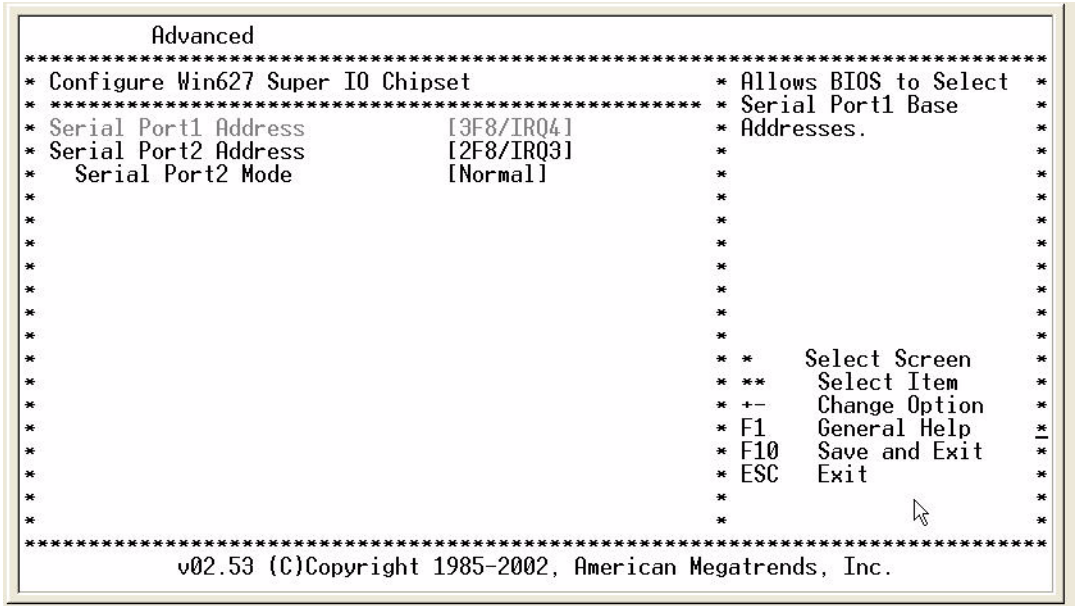


FIGURE B-5 Super IO Configuration Menu

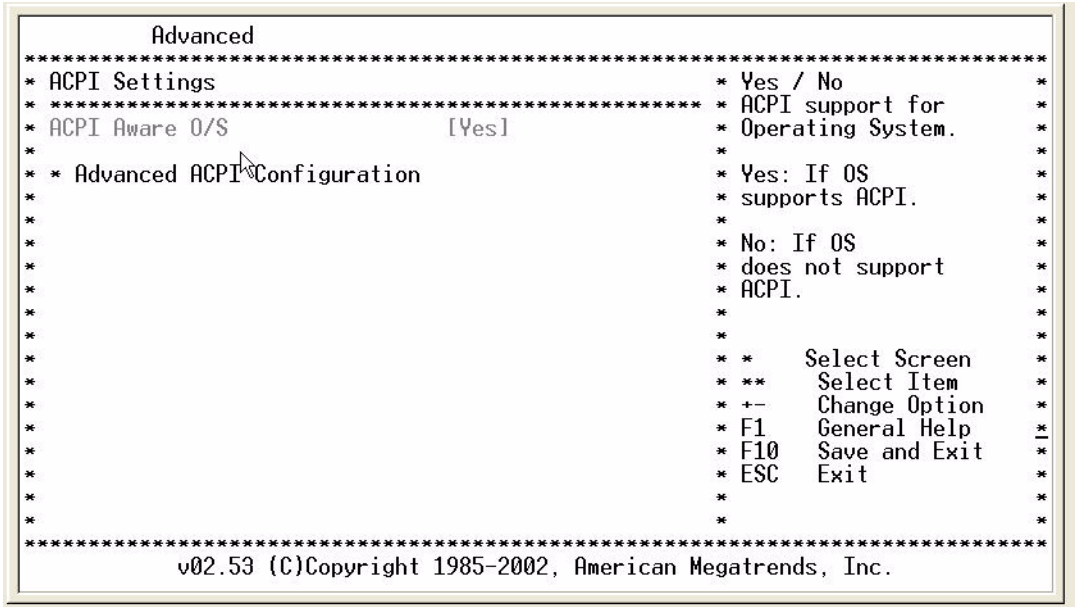


FIGURE B-6 ACPI Settings Menu

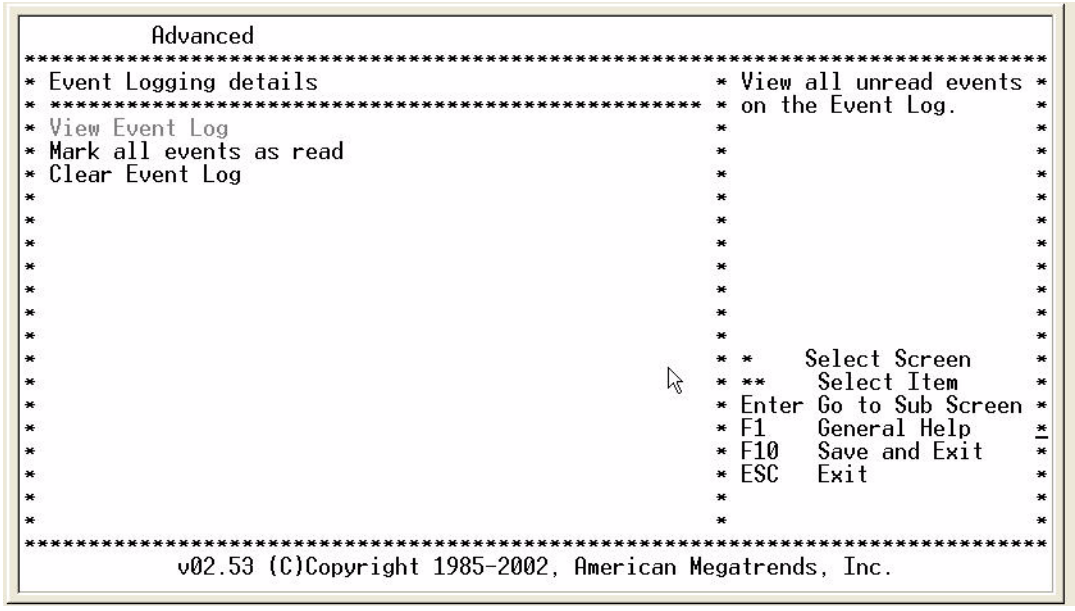


FIGURE B-7 Event Logging Details Menu

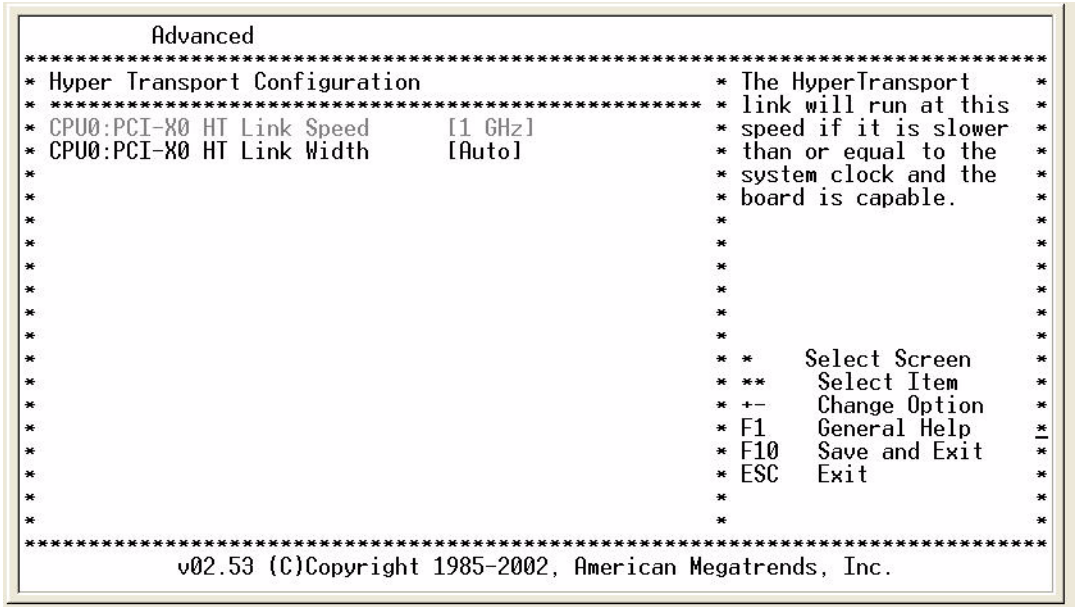


FIGURE B-8 Hyper Transport Configuration Menu

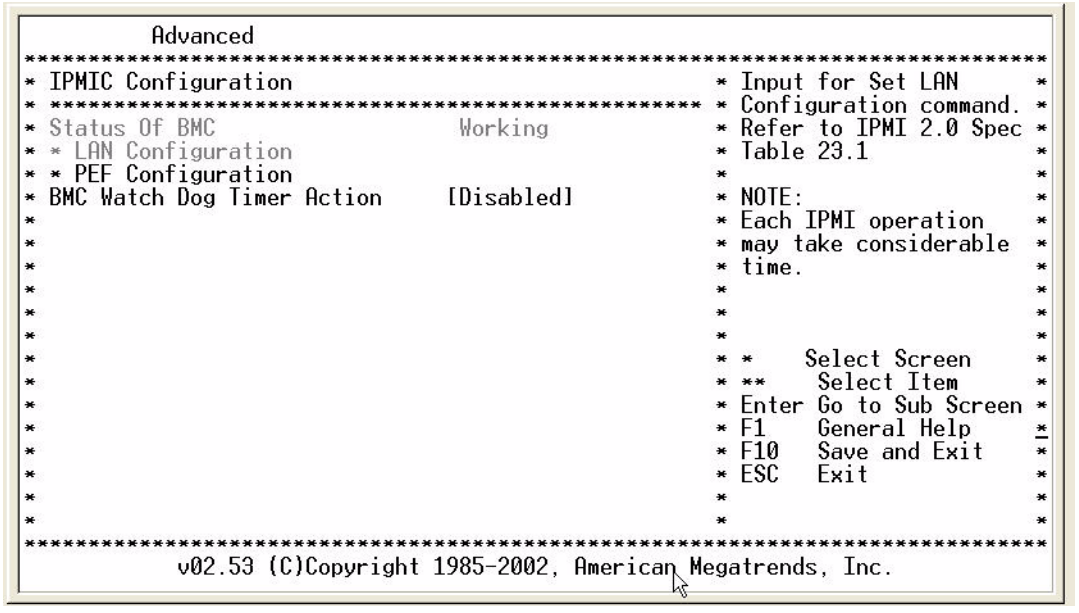


FIGURE B-9 IPMIC Configuration Menu

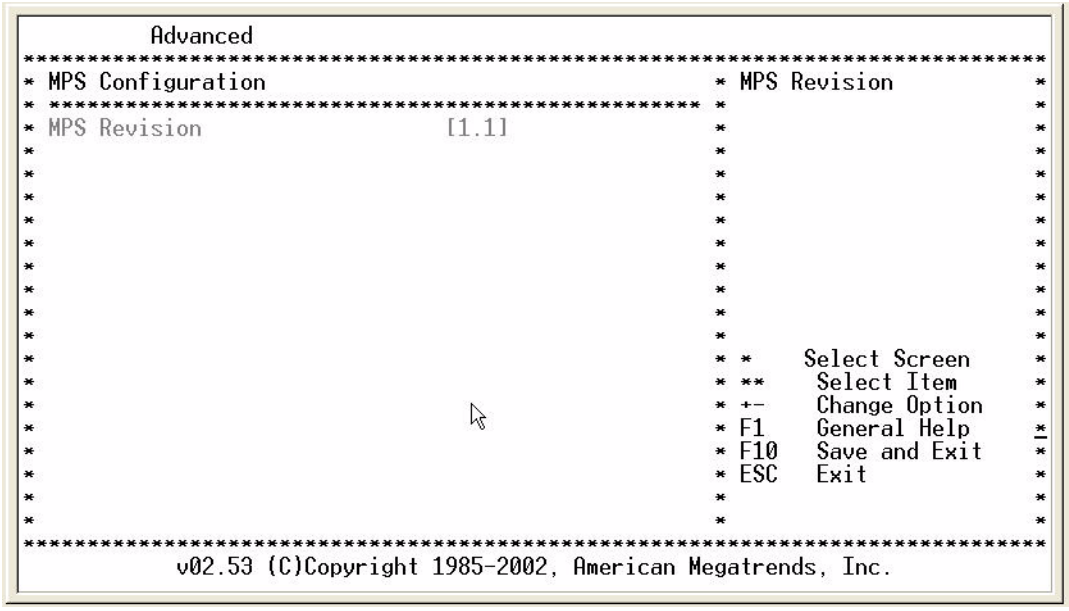


FIGURE B-10 MPS Configuration Menu

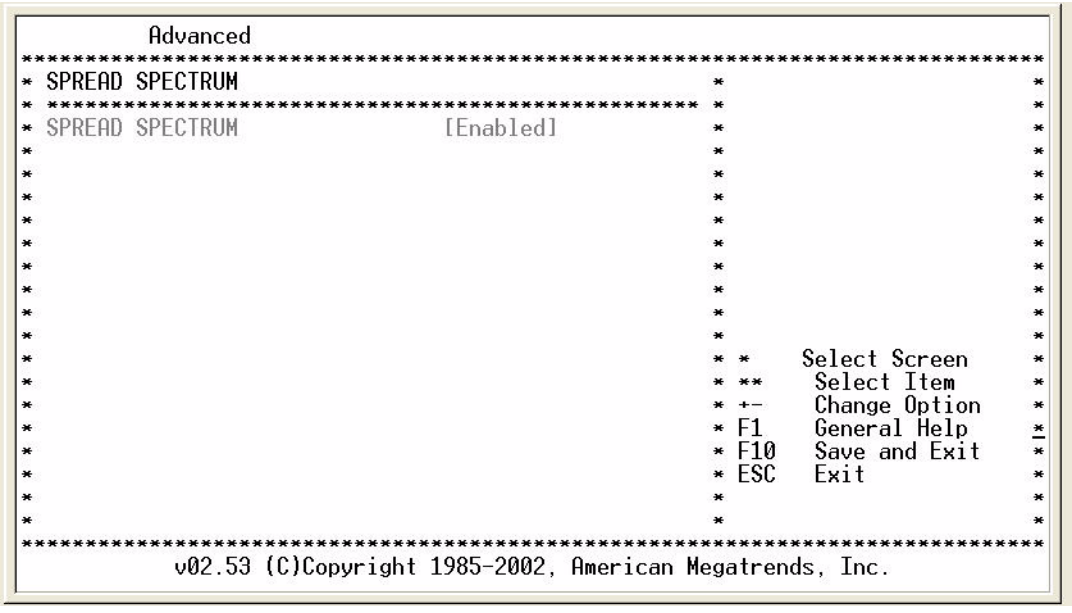


FIGURE B-11 Spread Spectrum Configuration Menu

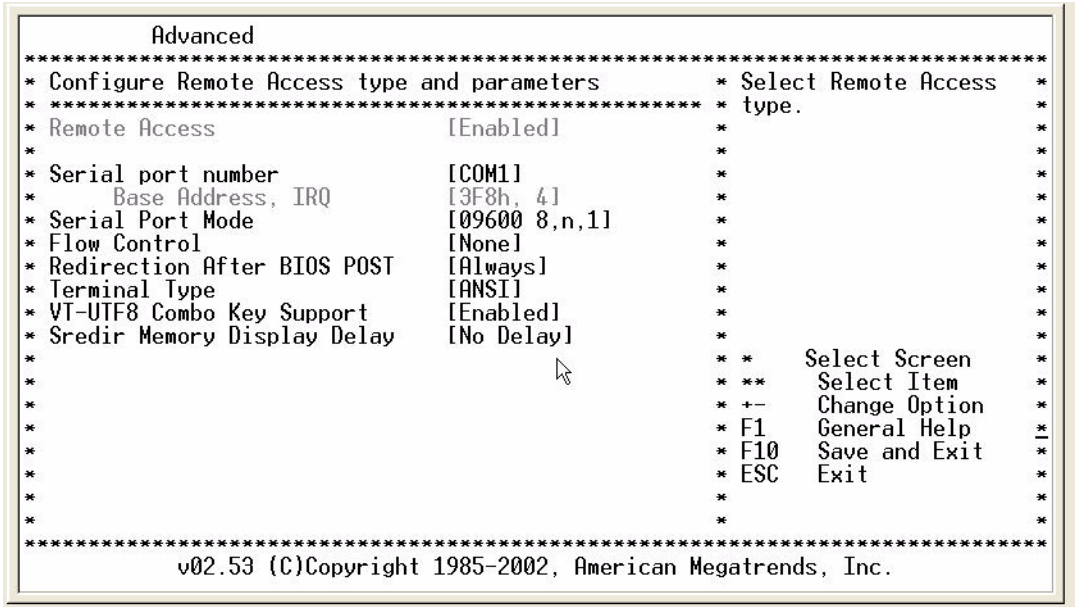


FIGURE B-12 Remote Access Configuration Menu

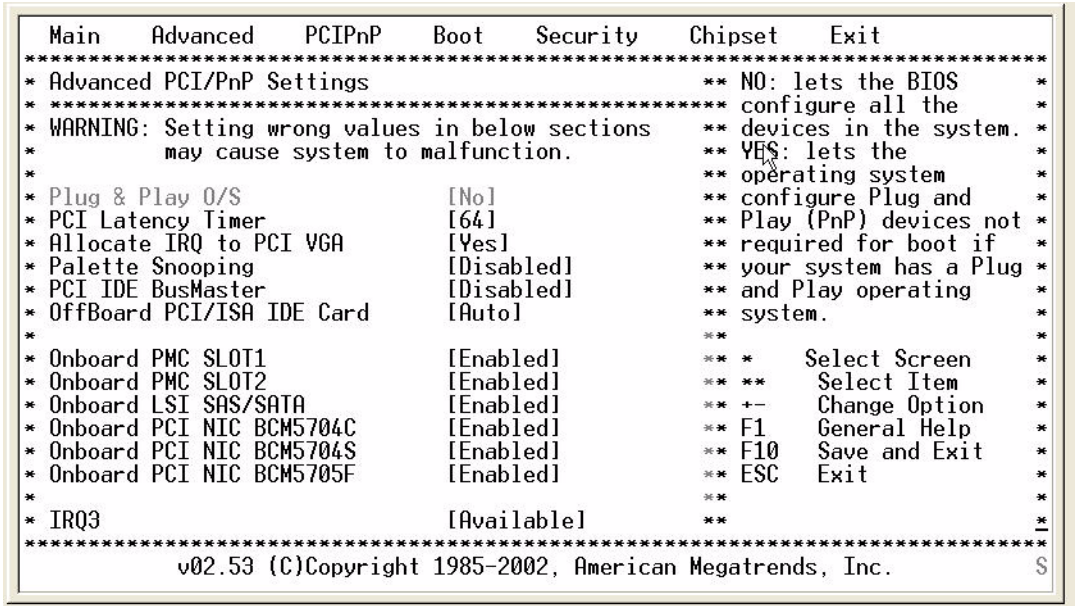


FIGURE B-13 Advanced PCI/PnP Settings Menu

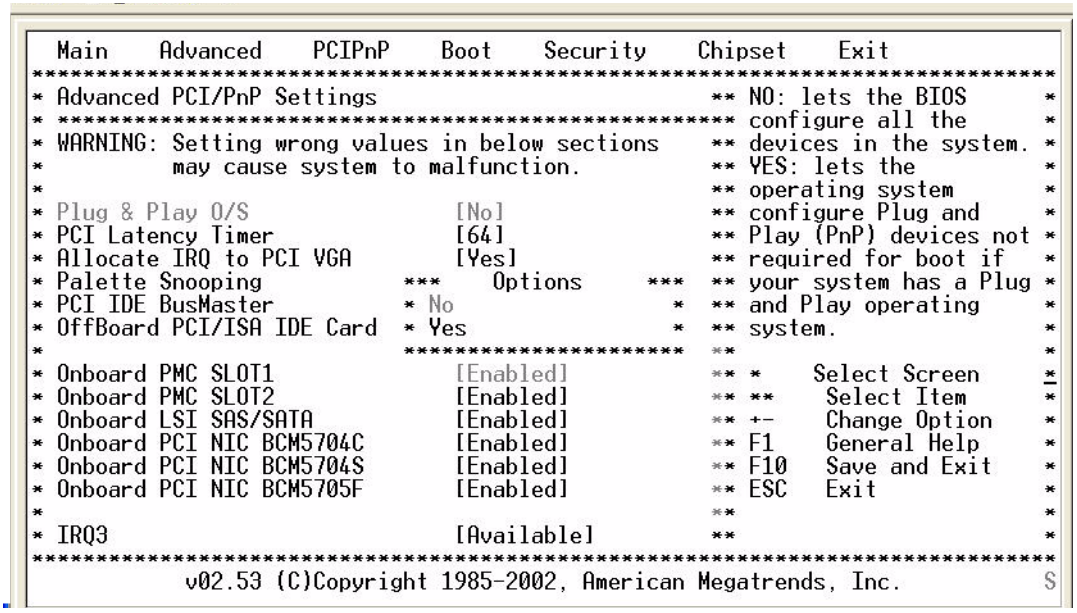


FIGURE B-14 Plug and Play Settings Menu

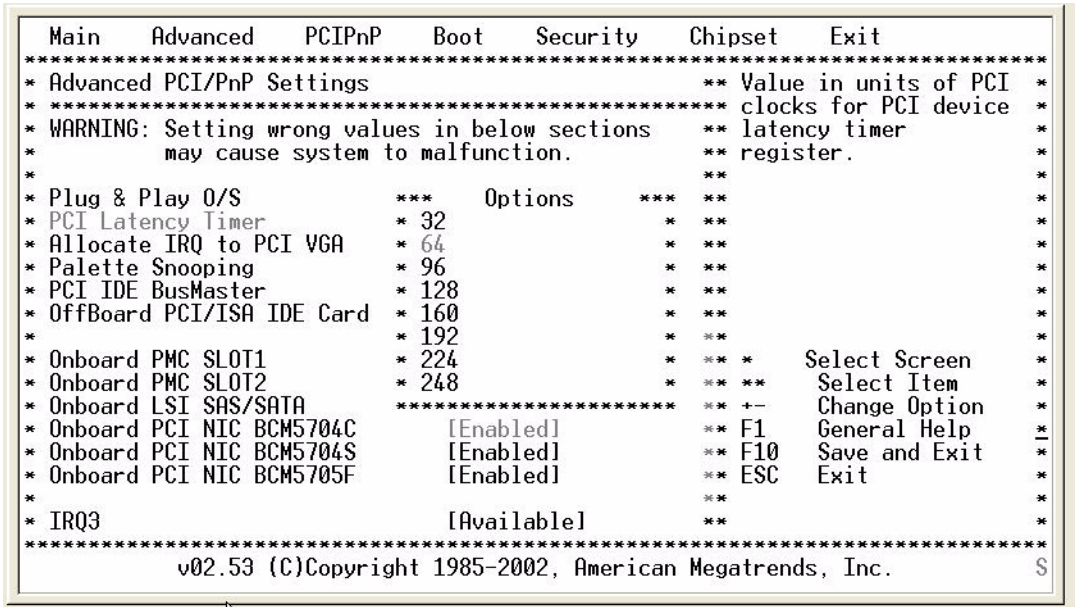


FIGURE B-15 PCI Latency Timer Settings Menu

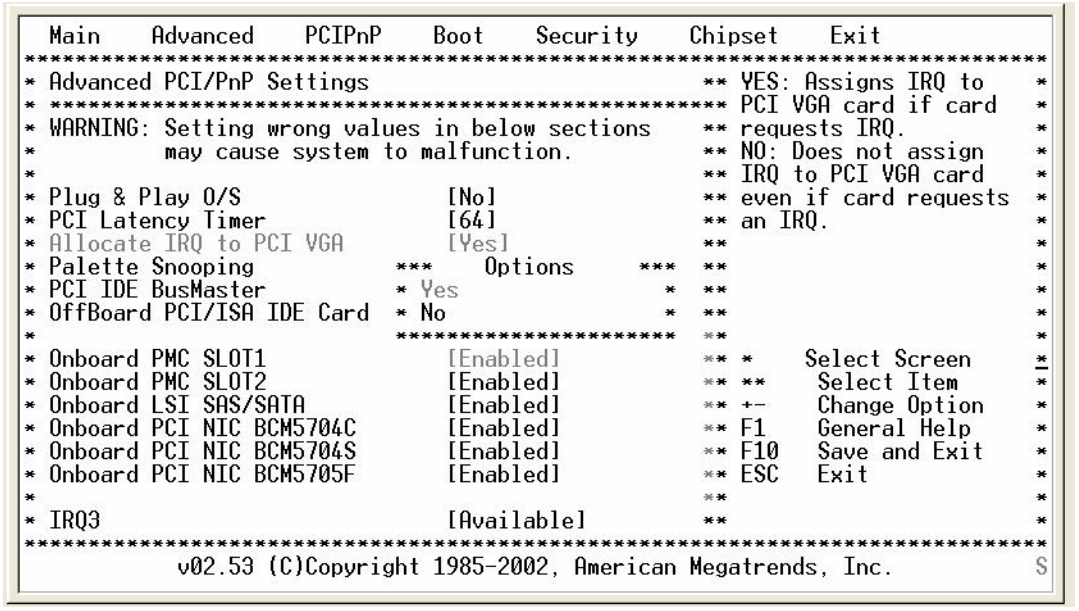


FIGURE B-16 Allocate IRQ to PCI VGA Settings Menu

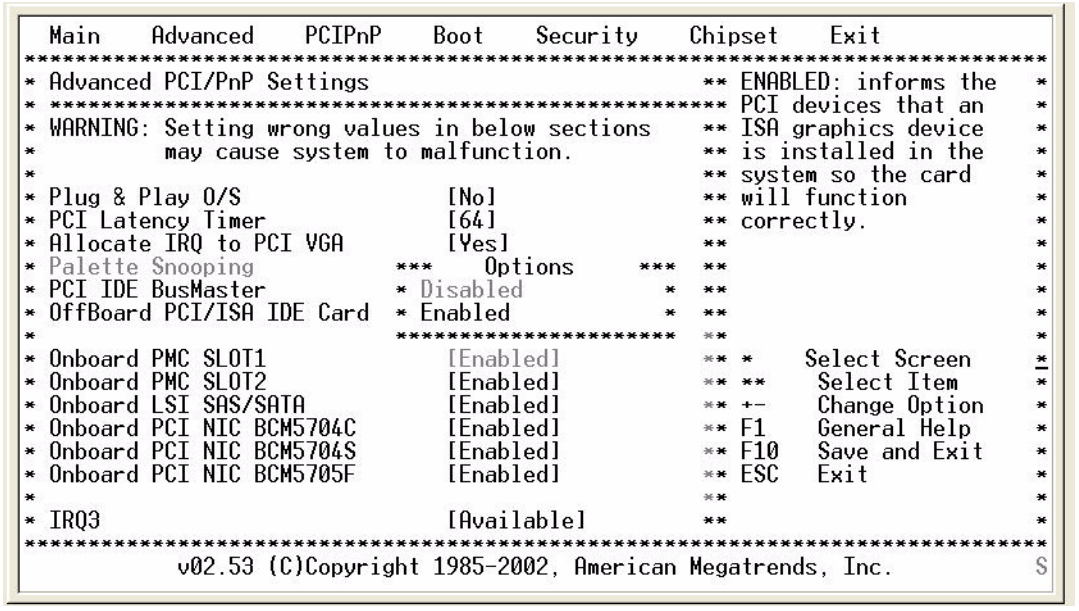


FIGURE B-17 Palette Snooping Settings Menu

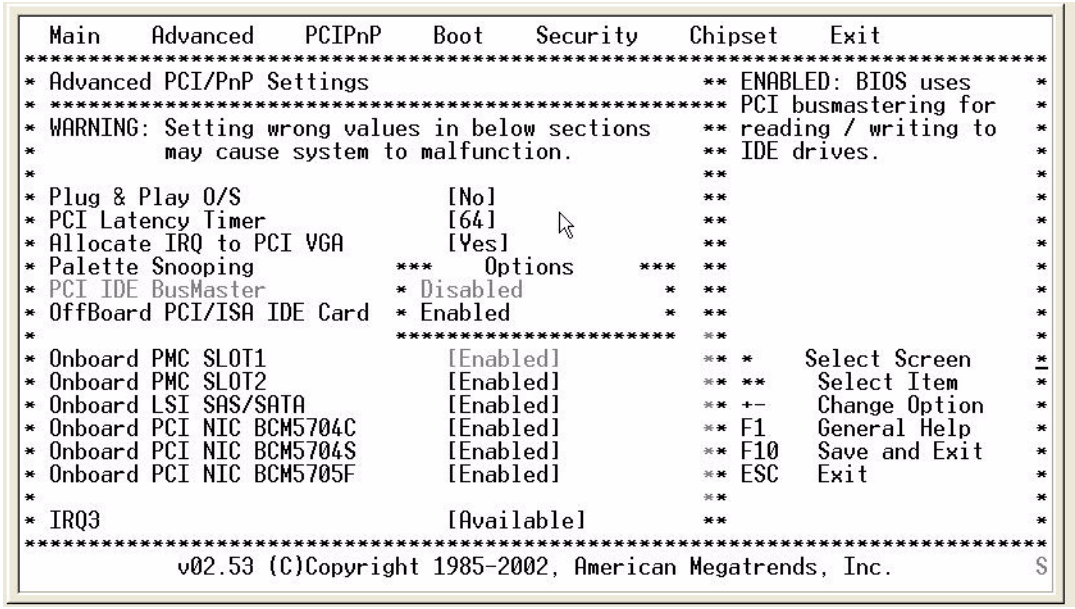


FIGURE B-18 PCI IDE BusMaster Settings Menu

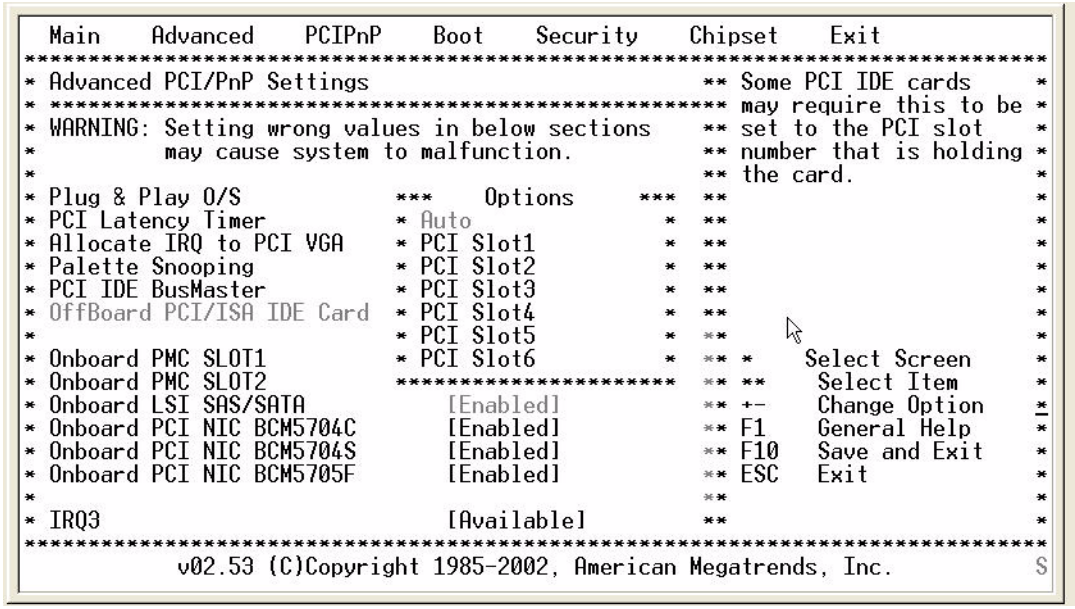


FIGURE B-19 OffBoard PCI/ISA IDE Card Settings Menu

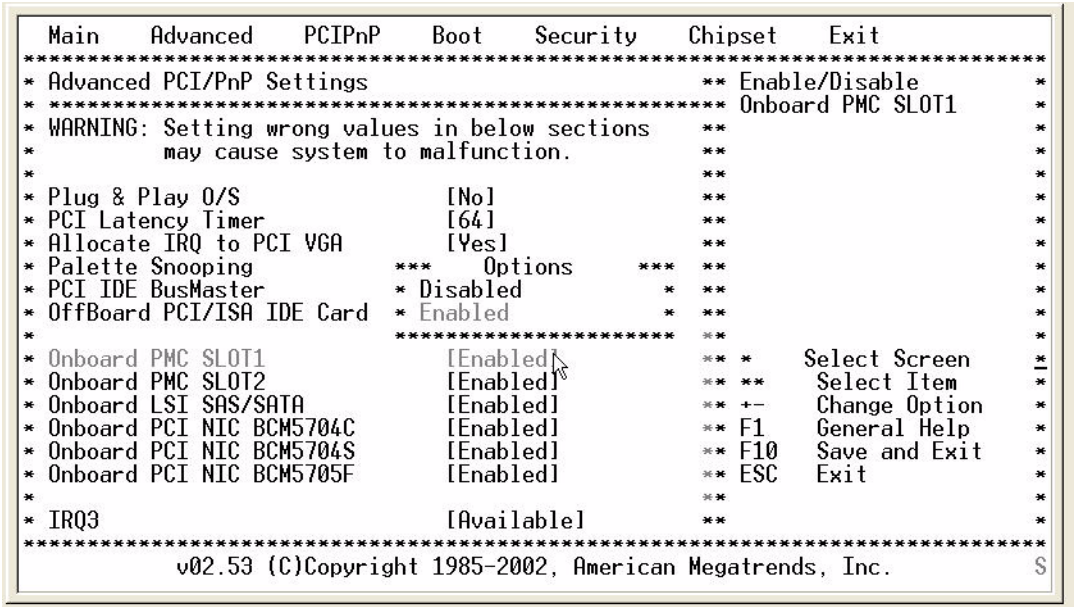


FIGURE B-20 Onboard PMC Slot1 Settings Menu

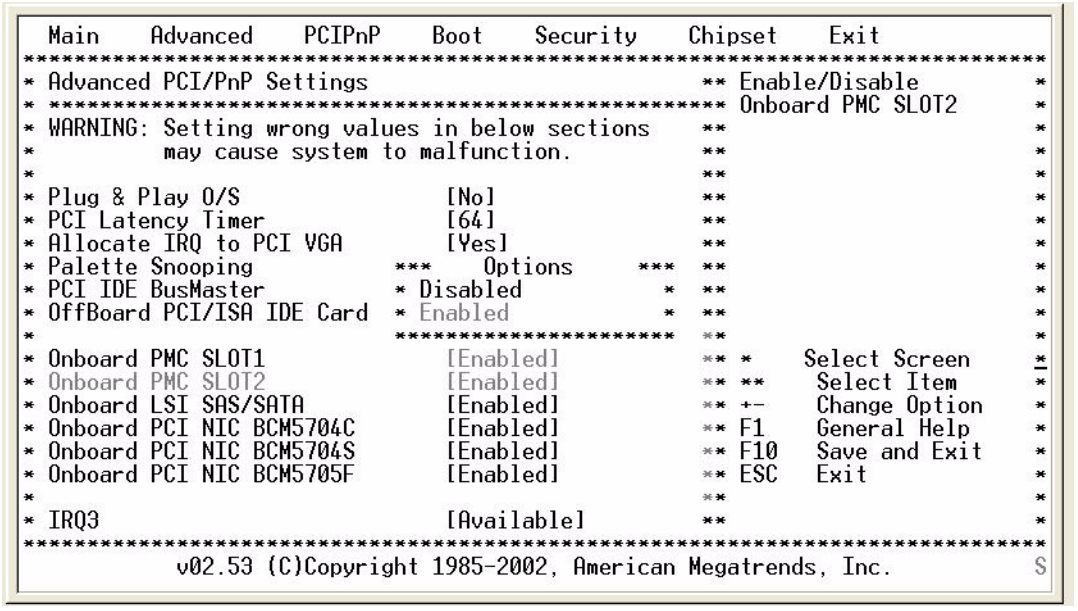


FIGURE B-21 Onboard PMC Slot2 Settings Menu

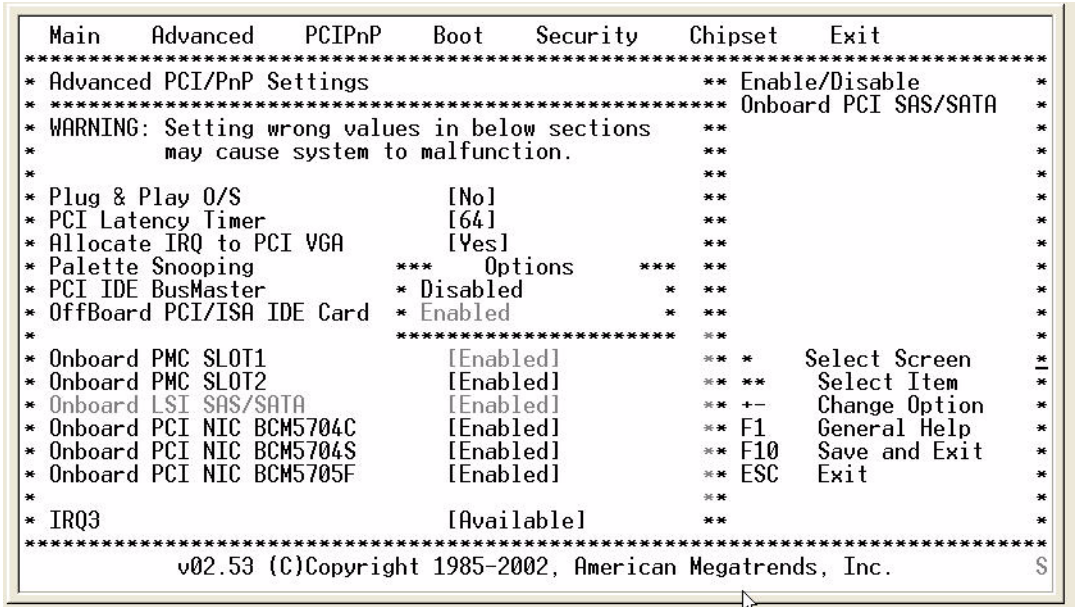


FIGURE B-22 Onboard LSI SAS/SATA Settings Menu

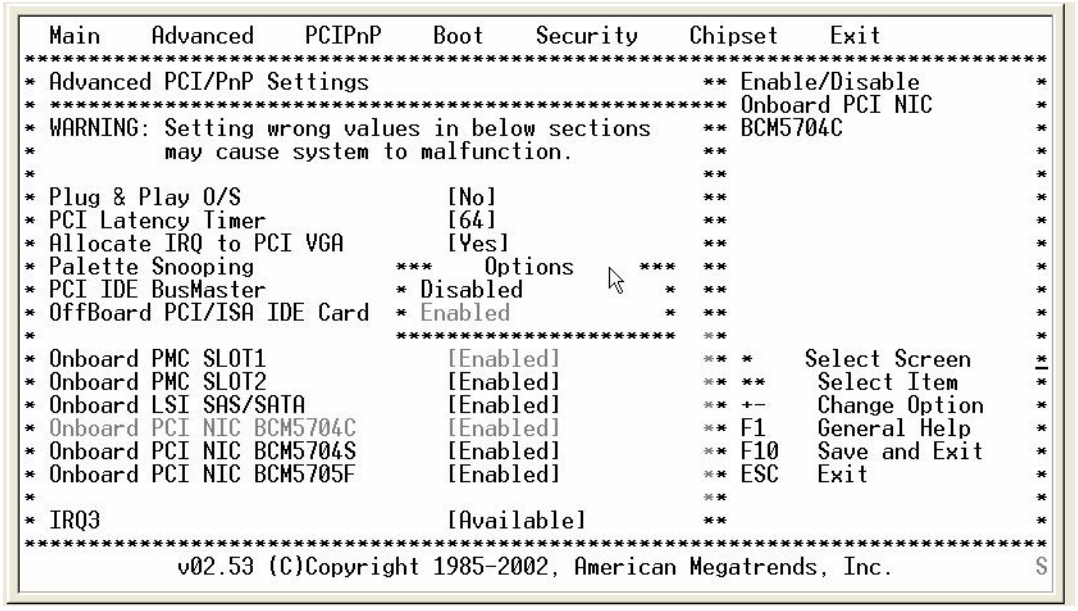


FIGURE B-23 Onboard PCI NIC BCM5704C Settings Menu

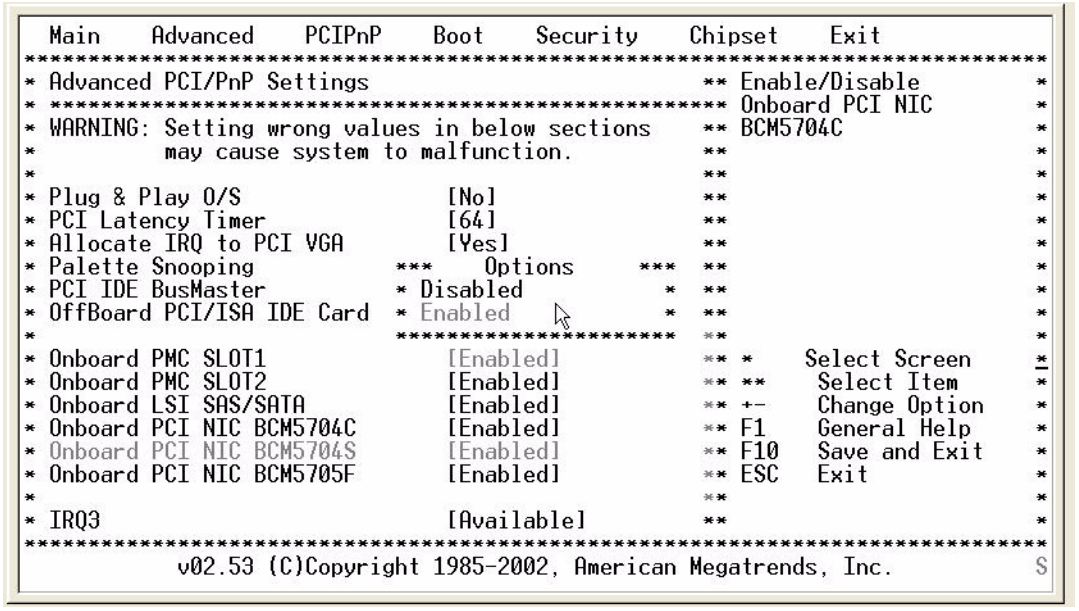


FIGURE B-24 Onboard PCI NIC BCM 5704S Settings Menu

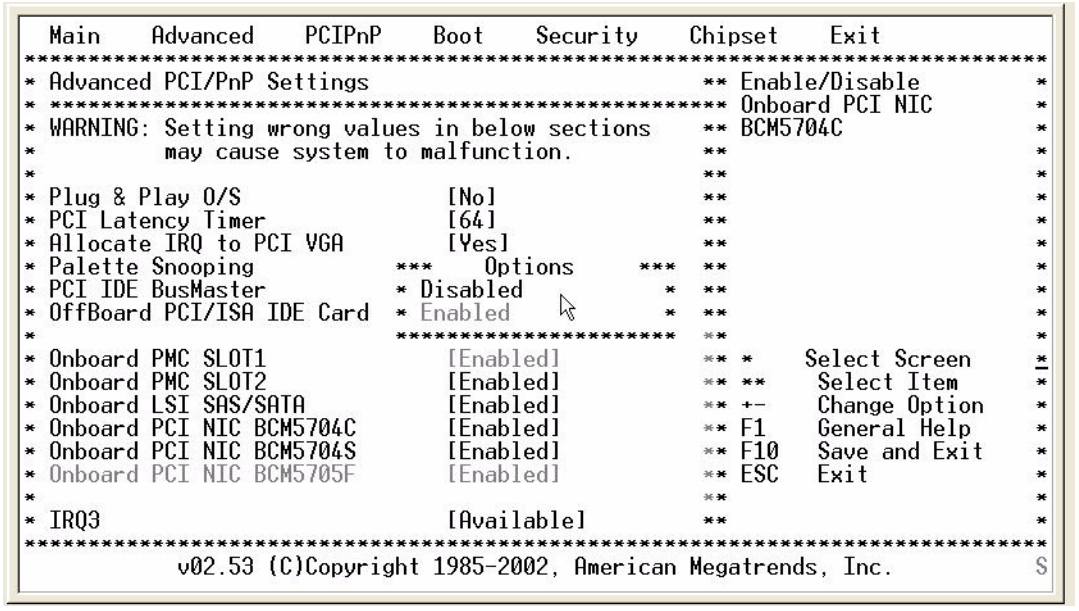


FIGURE B-25 Onboard PCI NIC BCM5705F Settings Menu

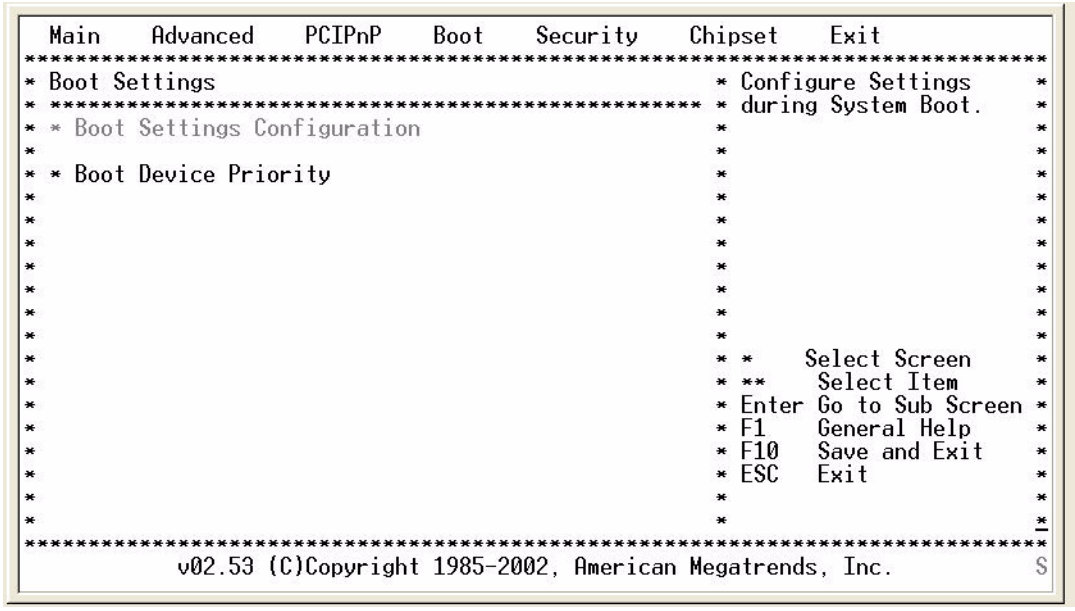


FIGURE B-26 Boot Settings Menu

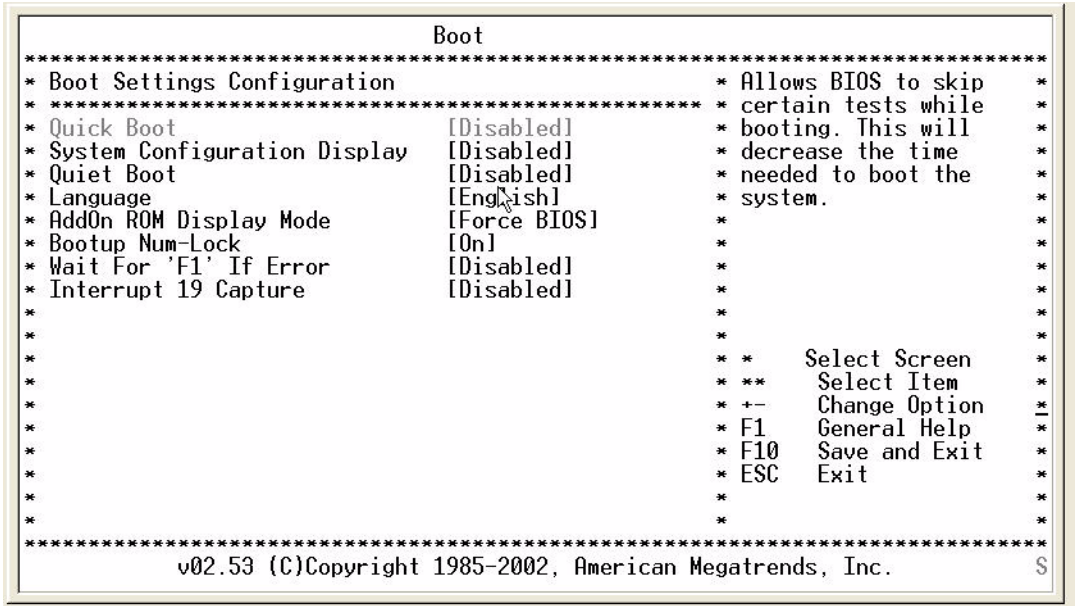


FIGURE B-27 Boot Settings Configuration Menu

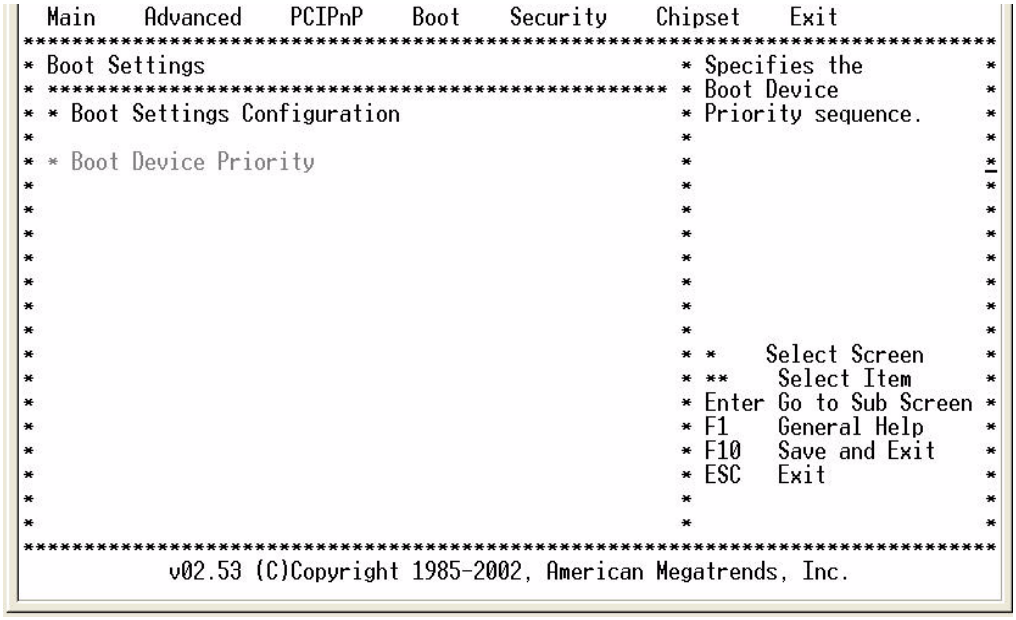


FIGURE B-28 Boot Device Priority Menu

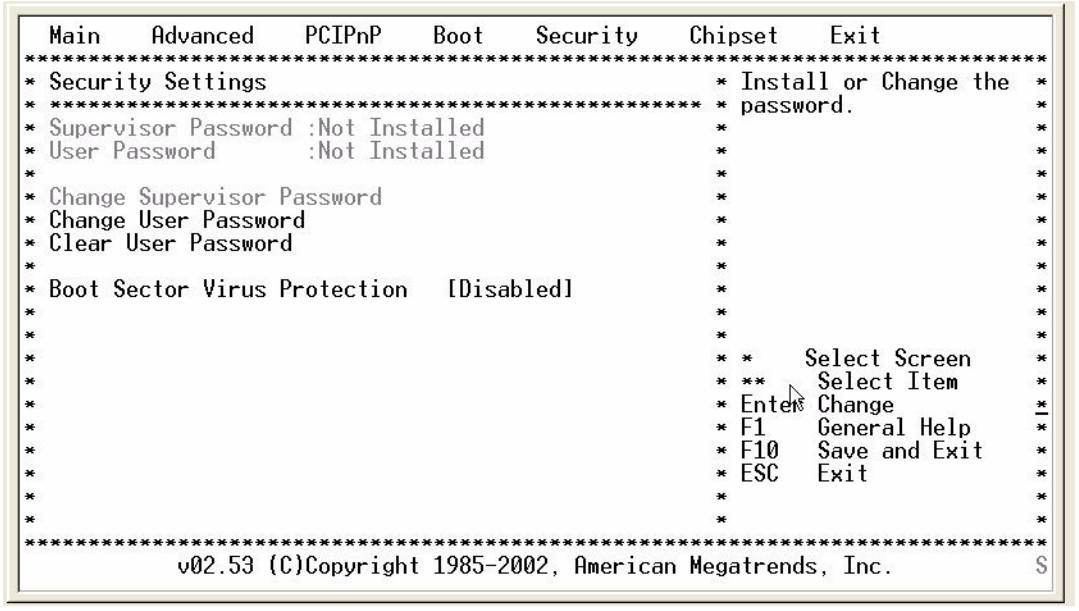


FIGURE B-29 Security Settings Menu

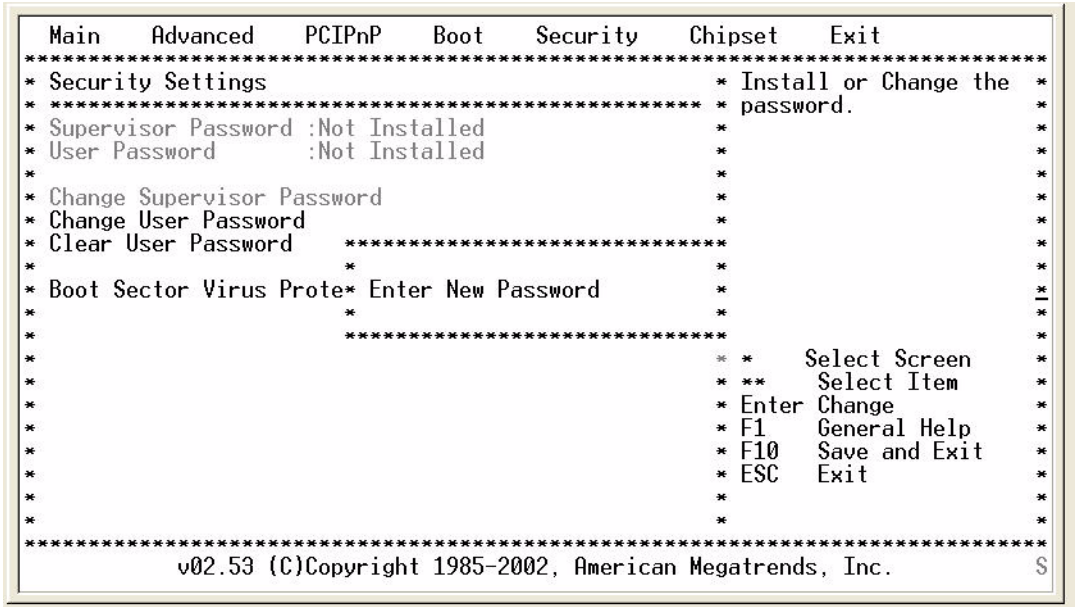


FIGURE B-30 Change Supervisor Password Settings Menu

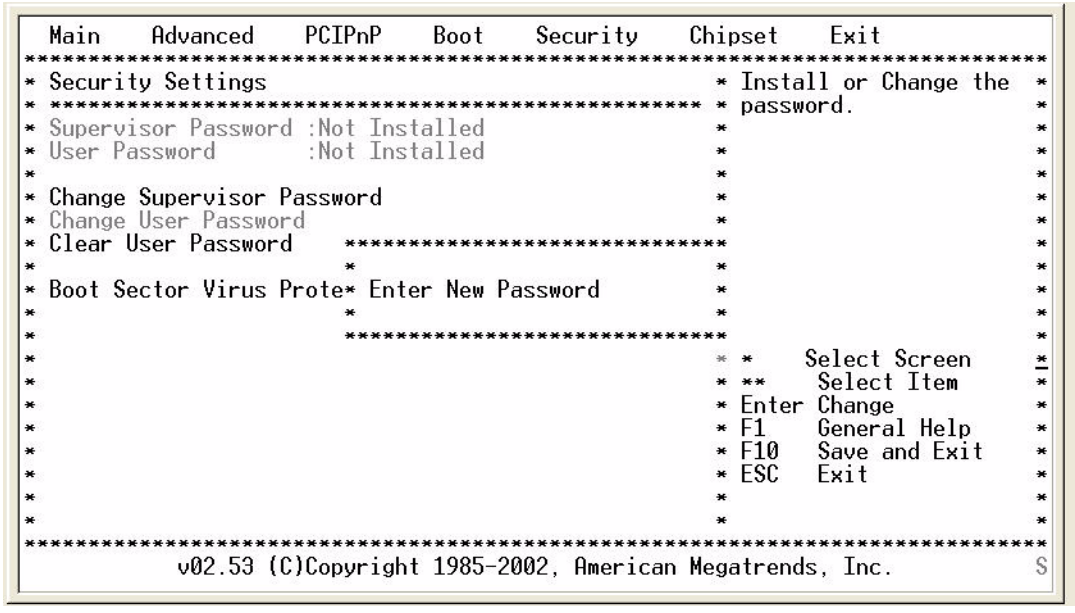


FIGURE B-31 Change User Password Settings Menu

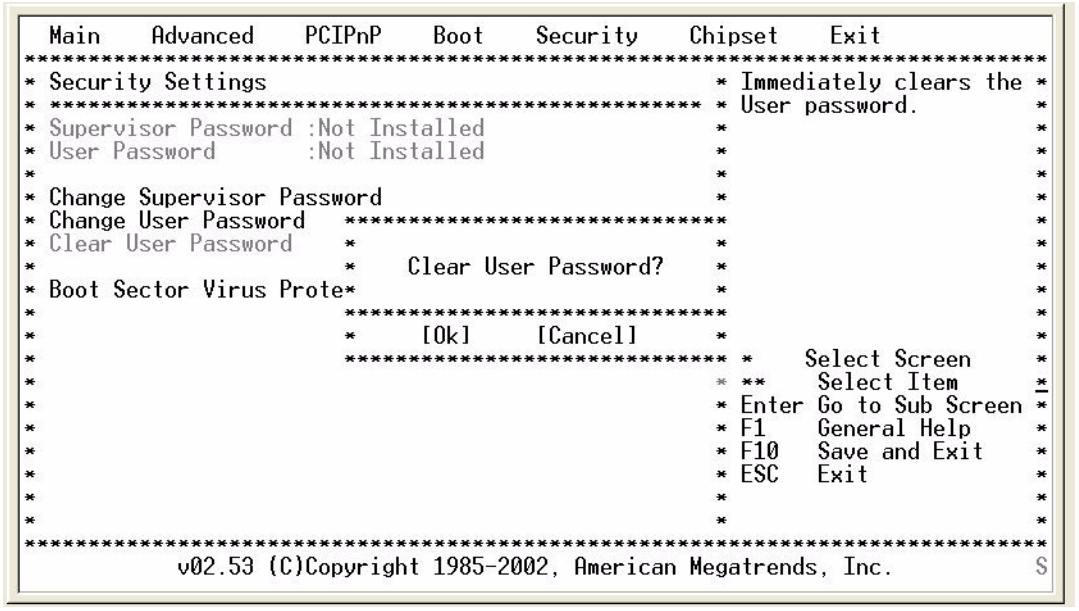


FIGURE B-32 Clear User Password Settings Menu

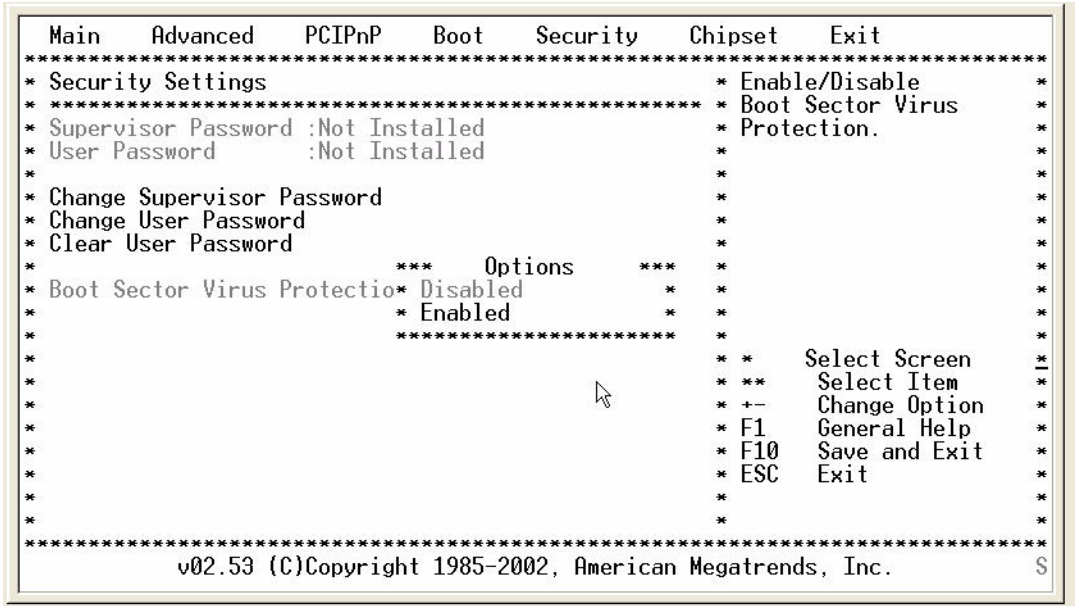


FIGURE B-33 Boot Sector Virus Protection Settings Menu

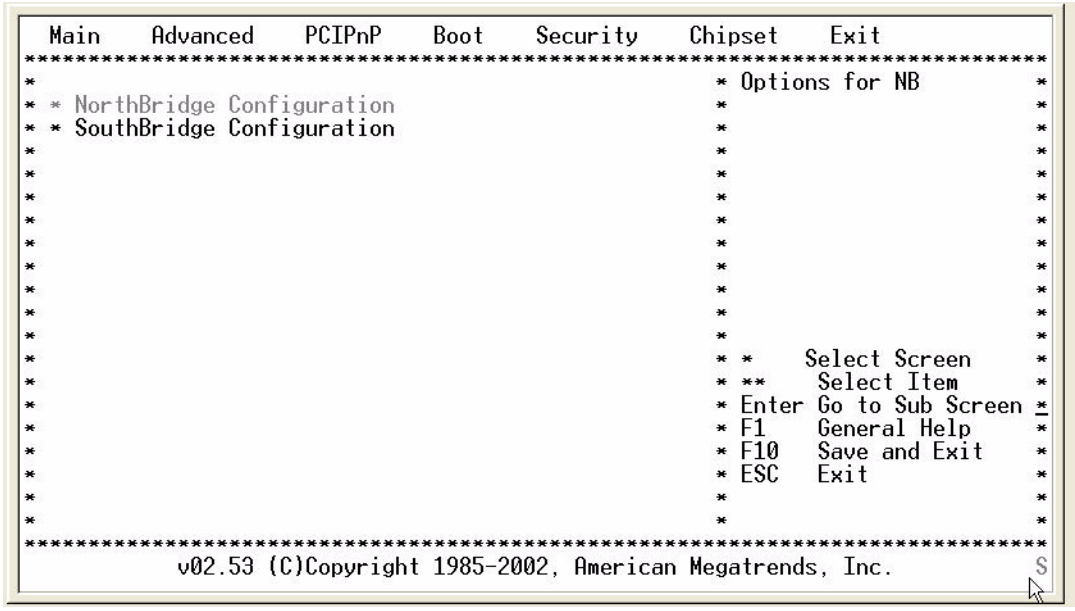


FIGURE B-34 Chipset Main Menu

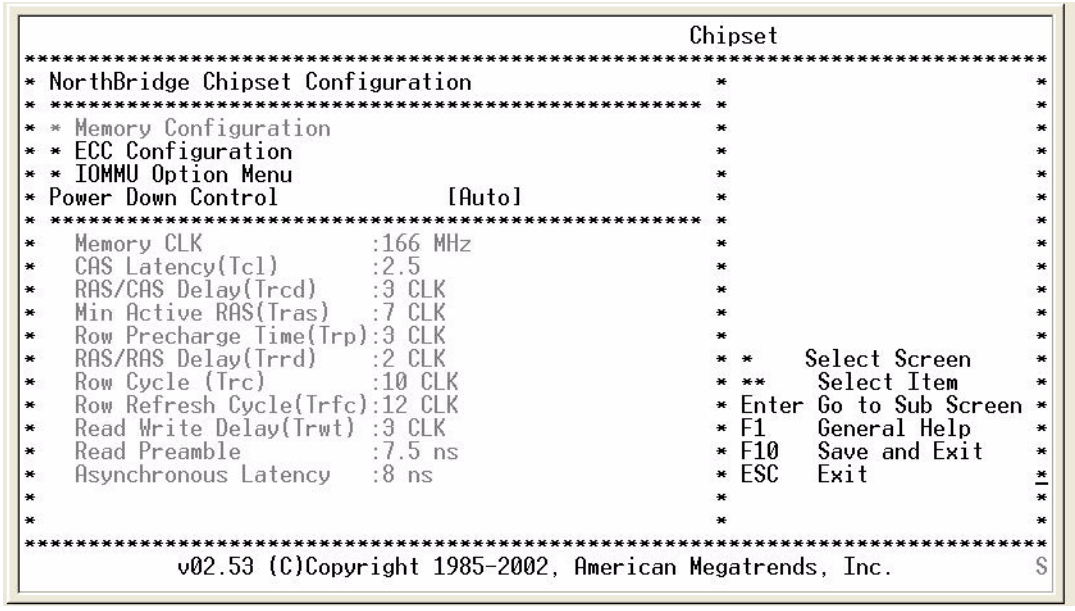


FIGURE B-35 NorthBridge Chipset Configuration Menu

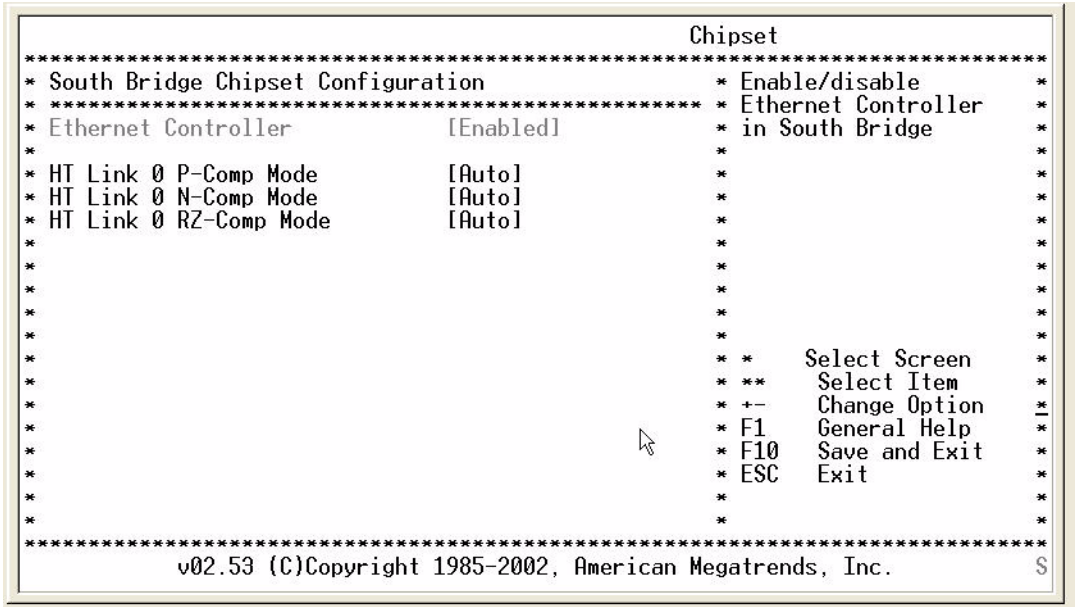


FIGURE B-36 SouthBridge Chipset Configuration Menu

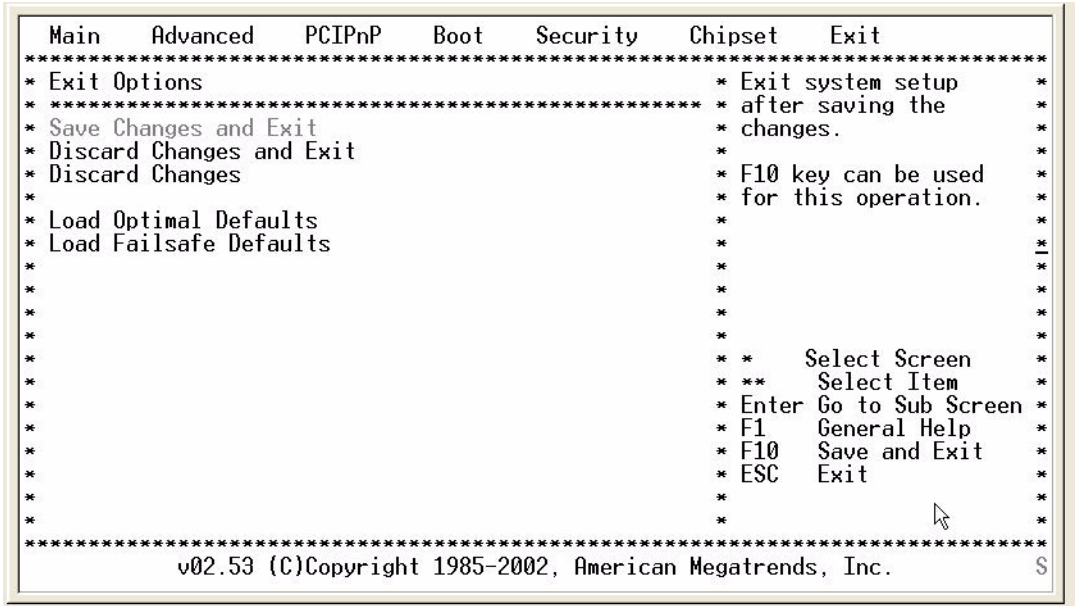


FIGURE B-37 Exit Options Menu

APPENDIX **C**

BIOS POST Codes

C.1 Power-On Self-Test (POST)

The system BIOS provides a rudimentary power-on self-test (POST). The basic devices required for the system to operate are checked, memory is tested, the LSI 1064 disk controller and attached disks are probed and enumerated, and the two Intel dual Gigabit Ethernet controllers are initialized.

The progress of the self-test is indicated by a series of POST codes.

These codes are displayed at the bottom right corner of the system's VGA screen (once the self-test has progressed far enough to initialize the video monitor). However, the codes are displayed as the self-test runs and scroll off of the screen too quickly to be read.

The message, `BMC Responding`, is displayed at the end of POST.

C.1.1 How BIOS POST Memory Testing Works

The BIOS POST memory testing is performed as follows:

1. **The first megabyte of DRAM is tested by the BIOS before the BIOS code is shadowed (that is, copied from ROM to DRAM).**
2. **Once executing out of DRAM, the BIOS performs a simple memory test (a write/read of every location with the pattern `55aa55aa`).**

Note – This memory test is performed only if Quick Boot is not enabled from the Boot Settings Configuration menu. Enabling Quick Boot causes the BIOS to skip the memory test. See Section C.1.2, "Changing POST Options" on page C-2 for more information.

3. **The BIOS polls the memory controllers for both correctable and noncorrectable memory errors and logs those errors into the service processor.**

C.1.2 Changing POST Options

These instructions are optional, but you can use them to change the operations that the server performs during POST testing.

1. **Initialize the BIOS Setup utility by pressing the F2 key while the system is performing the power-on self-test (POST).**
2. **When the BIOS Main Menu screen is displayed, select the Boot menu.**
3. **From the Boot Settings screen, select Boot Settings Configuration.**
4. **On the Boot Settings Configuration screen (**FIGURE B-27**), there are several options that you can enable or disable.**
   - Quick Boot – This option is disabled by default. If you enable Quick Boot, the BIOS skips certain tests while booting, such as the extensive memory test. This decreases the time it takes for the system to boot.
   - System Configuration Display – This option is disabled by default. If you enable this option, the system configuration screen is displayed before booting begins.
   - Quiet Boot – This option is disabled by default. If you enable this, the Sun Microsystems logo is displayed instead of POST codes.
   - Language – This option is reserved for future use. Do not change.
   - AddOn ROM Display Mode – This option is set to Force BIOS by default. This option has effect only if you have also enabled the Quiet Boot option, but it controls whether output from the Option ROM is displayed. The two settings for this option are as follows:
     - Force BIOS – Remove the Sun logo and display Option ROM output.
     - Keep Current – Do not remove the Sun logo. The Option ROM output is not displayed.
   - Bootup Num-Lock – This option is On by default (keyboard Num-Lock is turned on during boot). If you set this to off, the keyboard Num-Lock is not turned on during boot.
   - Wait for 'F1' If Error – This option is disabled by default. If you enable this, the system will pause if an error is found during POST and will only resume when you press the F1 key.

- Interrupt 19 Capture – This option is reserved for future use. Do not change.

C.1.3 POST Codes

TABLE C-1 contains descriptions of the POST codes, listed in the same order in which they are generated. These POST codes appear as a four-digit string that is a combination of two-digit output from primary I/O port 80 and two-digit output from secondary I/O port 81. In the POST codes listed in TABLE C-1, the first two digits are from port 81 and the last two digits are from port 80.

TABLE C-1 POST Codes

Post Code	Description
00d0	Coming out of POR, PCI configuration space initialization, Enabling 8111's SMBus.
00d1	Keyboard controller BAT, Waking up from PM, Saving power-on CPUID in scratch CMOS.
00d2	Disable cache, full memory sizing, and verify that flat mode is enabled.
00d3	Memory detections and sizing in boot block, cache disabled, IO APIC enabled.
01d4	Test base 512KB memory. Adjust policies and cache first 8MB.
01d5	Boot block code is copied from ROM to lower RAM. BIOS is now executing out of RAM.
01d6	Key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If next code is E0, BIOS recovery is being executed. Main BIOS checksum is tested.
01d7	Restore CPUID; moving boot block-runtime interface module to RAM; determine whether to execute serial flash.
01d8	Decompress runtime module into RAM. Storing CPUID information in memory.
01d9	Copy main BIOS into memory.
01da	Give control to BIOS POST.
0004	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. If the CMOS checksum is bad, update CMOS with power-on default values.
00c2	Set up boot strap processor for POST. This includes frequency calculation, loading BSP microcode, and applying user requested value for GART Error Reporting setup question.
00c3	Errata workarounds applied to the BSP (#78 & #110).

TABLE C-1 POST Codes *(Continued)*

Post Code	Description
00c6	Re-enable cache for boot strap processor and apply workarounds in the BSP for errata #106, #107, #69, and #63 if appropriate.
00c7	HT sets link frequencies and widths to their final values.
000a	Initialize the 8042 compatible Keyboard Controller.
000c	Detect the presence of Keyboard in KBC port
000e	Test and initialize different Input Devices. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1.
8600	Prepare CPU for booting to OS by copying all of the context of the BSP to all application processors present. Note: APs are left in the CLI HLT state.
de00	Prepare CPU for booting to OS by copying all of the context of the BSP to all application processors present. Note: APs are left in the CLI HLT state.
8613	Initialize PM regs and PM PCI regs at Early-POST. Initialize multi host bridge, if system supports it. Setup ECC options before memory clearing. Enable PCI-X clock lines.
0024	Decompress and initialize any platform specific BIOS modules.
862a	BBS ROM initialization.
002a	Generic Device Initialization Manager (DIM)–Disable all devices.
042a	ISA PnP devices–Disable all devices.
052a	PCI devices–Disable all devices.
122a	ISA devices–Static device initialization.
152a	PCI devices–Static device initialization.
252a	PCI devices–Output device initialization.
202c	Initialize different devices. Detect and initialize the video adapter installed in the system that have optional ROMs.
002e	Initialize all the output devices.
0033	Initialize the silent boot module. Set the window for displaying text information.
0037	Display sign-on message, CPU information, setup key message, and any OEM specific information.

TABLE C-1 POST Codes *(Continued)*

Post Code	Description
4538	PCI devices–IPL device initialization.
5538	PCI devices–General device initialization.
8600	Prepare CPU for booting to OS by copying all of the context of the BSP to all application processors present. Note: APs are left in the CLI HLT state.

C.1.4 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. TABLE B-2 describes the type of checkpoints that might occur during the POST portion of the BIOS. These two-digit checkpoints are the output from primary I/O port 80.

TABLE C-2 POST Code Checkpoints

Post Codes	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. At this point, only ROM accesses are to the GPNV. If BB size is 64K, require to turn on ROM Decode below FFFF0000h. It should allow USB to run in E000 segment. The HT must program the NB specific initialization and OEM specific initialization can program it if need at beginning of BIOS POST, like overriding the default values of Kernel Variables.
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initialize data variables that are based on CMOS setup questions. Initialize both the 8259 compatible PICs in the system.
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to POSTINT1ChHandlerBlock.
C0	Early CPU Init Start–Disable Cache–Init Local APIC.
C1	Set up boot strap processor information.
C2	Set up boot strap processor for POST. This includes frequency calculation, loading BSP microcode, and applying user requested value for GART Error Reporting setup question.
C3	Errata workarounds applied to the BSP (#78 & #110).
C5	Enumerate and set up application processors. This includes microcode loading, and workarounds for errata (#78, #110, #106, #107, #69, #63).

TABLE C-2 POST Code Checkpoints *(Continued)*

Post Codes	Description
C6	Re-enable cache for boot strap processor, and apply workarounds in the BSP for errata #106, #107, #69, and #63 if appropriate. In case of mixed CPU steppings, errors are sought and logged, and an appropriate frequency for all CPUs is found and applied. Note: APs are left in the CLI HLT state.
C7	The HT sets link frequencies and widths to their final values. This routine gets called after CPU frequency has been calculated to prevent bad programming.
0A	Initialize the 8042 compatible Keyboard Controller.
0B	Detect the presence of PS/2 mouse.
0C	Detect the presence of Keyboard in KBC port.
0E	Test and initialize different Input Devices. Also, update the kernel variables. Trap the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Decompress all available language, BIOS logo, and Silent logo modules.
13	Initialize PM regs and PM PCI regs at Early-POST. Initialize multi host bridge, if system supports it. Setup ECC options before memory clearing. REDIRECTION causes corrected data to be written to RAM immediately. CHIPKILL provides 4 bit error detection correction of x4 type memory. Enable PCI-X clock lines in the 8131.
20	Relocate all the CPUs to a unique SMBASE address. The BSP will be set to have its entry point at A000:0. If fewer than 5 CPU sockets are present on a board, subsequent CPU entry points will be separated by 8000h bytes. If more than 4 CPU sockets are present, entry points are separated by 200h bytes. CPU module will be responsible for the relocation of the CPU to correct address. Note: APs are left in the INIT state.
24	Decompress and initialize any platform-specific BIOS modules.
30	Initialize System Management Interrupt.
2A	Initialize different devices through DIM.
2C	Initialize different devices. Detect and initialize the video adapter installed in the system that have optional ROMs.
2E	Initialize all the output devices.
31	Allocate memory for ADM module and decompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initialize the silent boot module. Set the window for displaying text information.
37	Display sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initialize different devices through DIM.
39	Initialize DMAC-1 and DMAC-2.

TABLE C-2 POST Code Checkpoints *(Continued)*

Post Codes	Description
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	By this point, RAM read/write test is completed. Program memory holes or handle any adjustments needed in RAM size with respect to NB. Test if HT Module found an error in Boot Block and CPU compatibility for MP environment.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, etc.) successfully installed in the system and update the BDA, EBDA, etc.
50	Program the memory hole or any kind of implementation that needs an adjustment in system RAM size, if needed.
52	Update CMOS memory size from memory found in memory test. Allocate memory for Extended BIOS Data Area from base memory.
60	Initialize NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initialize IPL devices controlled by BIOS and option ROMs.
7C	Generate and write contents of ESCD in NVRAM.
84	Log errors encountered during POST.
85	Display errors to the user and get the user response for error.
87	Execute BIOS setup if needed/requested.
8C	After all device initialization is done, program any user selectable parameters relating to NB/SB, such as timing parameters, non-cacheable regions and the shadow RAM cacheability; and do any other NB/SB/PCIX/OEM specific programming needed during Late-POST. Background scrubbing for DRAM; L1 and L2 caches are set up based on setup questions. Get the DRAM scrub limits from each node. Work around for erratum #101 applied here.
8D	Build ACPI tables (if ACPI is supported).
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Take care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module.
A7	Display the system configuration screen if enabled. Initialize the CPUs before boot, which includes the programming of the MTRRs.

TABLE C-2 POST Code Checkpoints *(Continued)*

Post Codes	Description
A8	Prepare CPU for OS boot including final MTRR values.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitializes the ADM module.
AB	Prepare BBS for Int 19 boot.
AC	Any kind of Chipsets (NB/SB) specific programming needed during End- POST, just before giving control to runtime code booting to OS. Program the system BIOS (0F0000h shadow RAM) cache-ability. Port to handle any OEM-specific programming needed during End-POST. Copy OEM-specific data from POST_DSEG to RUN_CSEG.
B1	Save system context for ACPI.
00	Prepare CPU for booting to OS by copying all of the context of the BSP to all application processors present. Note: APs are left in the CLIHLT state.
61-70	OEM POST Error. This range is reserved for chipset vendors and system manufacturers. The error associated with this value may be different from one platform to the next.

Index

D

E

F

H

I

L

M

N

O

P

R

S

T

U

V

W